XM24LH

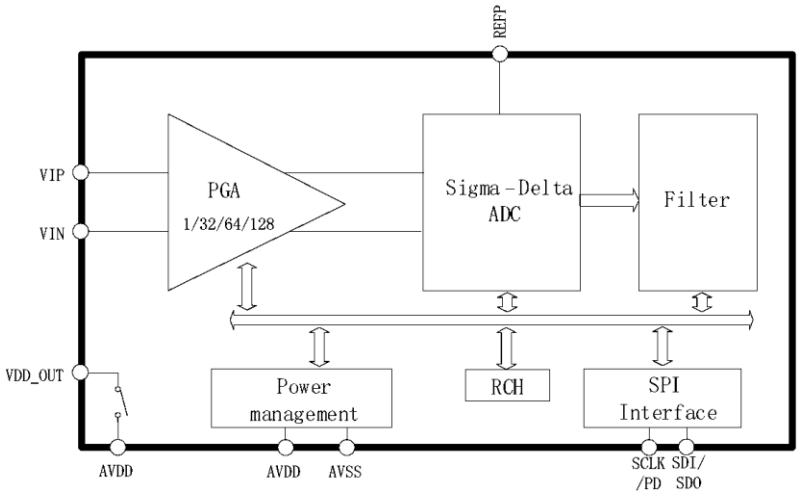
Features

- Voltage range:2.8~5.5V
- Current:
  - Normal mode: 1.5mA
  - Low power mode:0.7mA
  - Sleep mode:0.3uA
- Built-in programmable low-noise instrumental amplifier, 1/2/4/8/16/32/64/128 times
- 24-bit high-precision low offset Sigma-Delta ADC
  - Supporting 2 data rates, 10 Hz/20Hz
  - Linearity 0.001% FS;
  - Noise level: $11nV/\sqrt{Hz}$ @ 128 PGA
  - Offset: less than 5uV@ 64/128 PGA
- Integrated with a 3.9MHz internal high-frequency RC clock, with a drift of less than 1% within the temperature range of -40℃ to85℃
- Integrated with an internal 20ppm/℃ high-precision reference voltage. The default reference voltage is the external one.
- The built-in low resistance power switch can be used to control the bridge sensor to save power consumption.
- SPI
  - Supporting 2-wire SPI interface
  - Supporting up-to-2MHz communication clock
  - Supporting the CRC checksum protection
- Temperature range:-40~+85℃
- Storage temperature range:-40~+125℃

Packaging style: SOP8

Application

- Electronic scale
- Industrial Process Control
- DC/AC power measurement
- Ear thermometer
- Applications requiring high precision
- Applications requiring low zero drift



PGA@128 Data Rate@10Hz			
MODE	噪声	ENOB	Noise Free
0	0.036uV	20.0bit	17.5bit
1	0.047uV	19.7bit	17.2bit

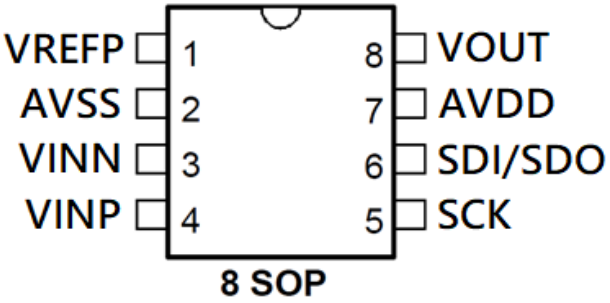
Summary

XM24LH is a single-channel, 24-bit high-precision ADC chip with a SPI interface, a built-in Gain 1/32/64/128 programmable low-noise instrumental amplifier and a high-precision Sigma Delta ADC, and it also integrates a high-frequency internal RC clock source inside.

The effective number of bits (ENOB) of ADC is 20 bit@128 PGA. Its equivalent input noise is as low as 11 nV/√Hz, the offset is 5uV.

It can be used in all kinds of weight scale, strain gauges , ear thermometer and other applications that requiring high precision and low offset.

晶片引腳



XM24LH 晶片引腳圖

PIN 腳說明

Pin	Name	Type	Description
1	VREFP	Input/Output	Positive input of reference voltage, connect a ceramic capacitor greater than or equal to 1uF between VREFP and AVSS. If config this chip’ s register to use internal reference, this pin is output mode and can’ t be connected to other voltage source.
2	AVSS	Ground	Gound
3	VINN	Input	Negative input of signal channel 0
4	VINP	Input	Positive input of signal channel 1
5	SCK	Input	SPI Input clock/PD signal If the SCK/PD pin’ s signal stays at ‘1’ for more than 100us, then the chip will turn to sleep mode. If the SCK/PD pin’ s signal stays at ‘0’ for more than 100us, then the chip will turn to work mode. In work mode, SCK is used to read the convert data, read SPI Interface chapter for detail. In sleep mode, SCK is used to read/write chip’ s register, read SPI Interface chapter for detail.
6	SDI/SDO	Input/Output	SPI Input data/SPI output data，there is 300k Ohm pull up resister from this pin to AVDD in this chip.
7	AVDD	Power	Power supply, connected a ceramic capacitor greater than or equal to 1uF between AVDD and AVSS
8	VOUT	Output	There is an internal switch connect this pin to AVDD. When the chip is in work mode, this switch is on, it can be connect to bride sensor’ s power side and VREFP. In sleep mode, this switch is off to save power.

1. AC and DC spec

1.1. Maximum ratings

When the external input or environmental parameters exceed the following conditions, it is likely to cause damage to the chip or shorten its service life. The following table only represents the scope of damage but not the scope of normal operation.

Table1-1 Maximum ratings

Symbol	Ratings	Min	Max	Unit
AVDD/DVDD	Power supply voltage	-0.3	+6	V
Vsig	Input signal	-0.3	+6	V
TS	Storage temperature	-50	+150	℃
TJ	Junction temperature under bias	-40	+125	℃

1.2. Parameters

Table1-2 Parameters

Symbol	Ratings	Min	Max	Unit	Symbol
AVDD/DVDD	IO voltage	2.8	5	5.5	V
IACTIVE	Current		1.5		mA
IPD	Sleep current		0.3		uA
VPOR	Power-on reset voltage	1.9	2	2.1	V
TA	Temperature range	-40	25	85	℃

1.3. ESD/LU performance

Table 1-3 ESD/Latch-Up performance

Symbol	Ratings	Min	Max	Unit
ESD(HBM)	ESD discharge voltage of HBM model	-4000	4000	V
Latch-Up	Latch-Up test current(@85℃)	-200	200	mA

1.4. GPIO parameters

Table1-4 GPIO parameters

Symbol	Ratings	Min	Max	Unit	Symbol	Ratings
VIH	High threshold of input signal	5V	4		5.5	V
VIL	Low threshold of input signal	5V	-0.3		1	V
VT+	Threshold of Schmidt from low to high voltage	5V	2.72	2.92	3.17	V
VT-	Threshold of Schmidt from high to low voltage	5V	1.85	2	2.17	V
IIH	Input of high level current	5V			+1	uA
IIL	Input of low level current	5V	-1			uA
VOL	Output of low level (@IOL current condition)	5V			0.4	V
VOH	Output of high level (@IOH current condition)	5V	4			V
IOL	Output of low-level current @VOL (max)	5V	4.9	8.8	13.9	mA
IOH	Output of high-level current @VOH (min)	5V	4.9	8.8	13.9	mA

1.5. ADC performance

Note: the following spec are all measured under AVDD= 5V,REFP=5V, unless otherwise specified

Table 1-5 ADC performance

Parameter	Min	Typ	Max	Unit
Precision				
Linearity		±0.001		%FS
ENOB		20@PGA=128 21.5@PGA=1		BIT
Noise Floor		11		nV/√Hz
Offset		500/PGA	640/PGA	uV
Offset drift		15	20	nV/℃
Gain error		0.6	0.8	%
Gain drift		3	4	ppm/℃
Input Signal				
Common mode range of input signals	AVSS		AVDD	V
Signals Range	$-REF2*GAIN$		$+REF2*GAIN$	REF=VREFP-REFN
Differential input currents		2		nA
Signal input impedance		>1G		Ω
CMRR		110		dB
Reference voltage				
VREFP	1		AVDD-AVSS	V
Built-in reference voltage	1.18	1.19	1.20	V
Temperature coefficient of built-in reference voltage		20		ppm/℃
Clock				
ADC converting rate(Data Rate)	10		20	Hz
Internal RC clock frequency	3.9-15%	3.9	3.9+15%	MHz
Power supply				
AVDD range	2.5	5	5.5	V
PSRR		110		dB
Current @normal mode		1.5@32/64/ 128PGA 0.31@1PGA		mA
Current @Low power mode		0.7@32/64/ 128PGA 0.31@1PGA		mA
Current @sleep mode		0.3		uA

1.5.1. MODE=0　ADC noise and ENOB

Note: the following spec are all measured under AVDD= 5V,REFP=5V, unless otherwise specified

Table 1-6　Equivalent input RMS noise (nV)

Data rate (Hz)	Noise (nV)@PGA (times)			
	128	64	32	1
10	0.036	0.042	0.061	1.629
20	0.051	0.060	0.086	2.304

Table 1-7ENOB

Data rate (Hz)	ENOB@PGA (times)			
	128	64	32	1
10	20.0	20.8	21.3	21.5
20	19.5	20.3	20.8	21.0

Table 1-8Noise Free Bits

數據碼率（Hz）	Noise Free Bits@PGA(times)			
	128	64	32	1
10	17.5	18.3	18.8	19.0
20	17.0	17.8	18.3	18.5

1.5.2. MODE=1　ADC noise and ENOB

Note: the following spec are all measured under AVDD= 5V,REFP=5V, unless otherwise specified

Table 1-9等效輸入RMS雜訊(uV)

Data rate (Hz)	Noise (nV)@PGA (times)			
	128	64	32	1
10	0.047	0.052	0.068	1.629
20	0.066	0.073	0.096	2.304

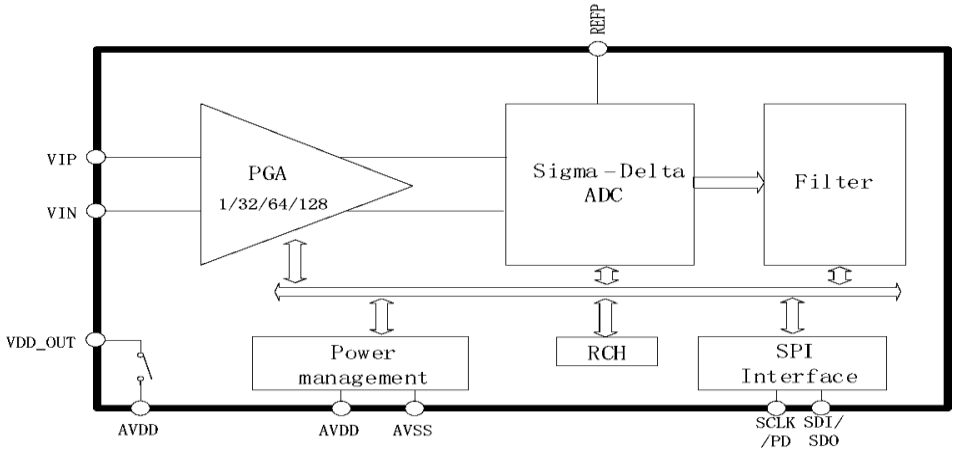
Table 1-10ENOB

Data rate (Hz)	ENOB@PGA (times)			
	128	64	32	1
10	19.7	20.5	21.1	21.5
20	19.2	20.0	20.6	21.0

Table 1-11Noise Free Bits

Data rate (Hz)	Noise Free Bits@PGA(times)			
	128	64	32	1
10	17.2	18.0	18.6	19.0
20	16.7	17.5	18.1	18.5

2 Description of modules



As shown in the figure above, the chip is comprised of a power management module, a high-frequency RCH clock, a BGP module, a programmable gain amplifier (PGA), a Sigma Delta ADC module, a digital filter module and an SPI interface module.

2.1. Power management module

The chip is powered by AVDD/AVSS, and the voltage range is 2.5 ~ 5.5V.

The power management module has an internal power-on reset (POR) circuit which provides a reset signal for the chip when power on.

The module also provides an internal MOS switch with a resistor of 10Ω to short the VDD_OUT pin to the AVDD pin. If the SCK/PD pin’ s signal stays at ‘0’ for more than 100us, then the chip will turn to work mode, and the switch will be on to power the bridge sensor and ADC’ s VREFP. If the SCK/PD pin’ s signal stays at ‘1’ for more than 100us, then the chip will turn to read/write mode and sleep mode. The switch will be off to save the power consumption of the bridge resistor.

2.2. High-frequency RCH clock

The chip is integrated with a 3.9MHz high frequency RCH clock.

The frequency drift of the RCH clock is less than 1% in the range of - 40 ~ 85 ℃, but the RCH frequency between chips has inherent deviation.

2.3. PGA電路

A 1/32/64/128 programmable high-precision instrumental amplifier is integrated in the chip, and the gain can be set through GA < 1:0 > in the register.

2.4. Sigma-Delta ADC

A high-performance Sigma-Delta ADC is integrated in the chip, the high-frequency bit stream generated by ADC is sent to the subsequent digital filter (DSP) circuit for processing, and then 24-bit ADC data are obtained.

2.5. Digital filter

The digital filter processes the high frequency bit stream generated by ADC conversion, and then 24-bit ADC data is obtained. The output frequency of the filter can be set as 10/20Hz through DR bit in the register.

2.6. Power mode

Set the SCK/PD pin to be ‘1(high)’ for more than 100us, then the chip will turn to read/write mode and sleep mode. In this mode, PGA/ADC/RCH/power switch will be turn off and the current is 0.3uA. But in this mode and only in this mode, the chip’ s config register can be read and write.

2.7. SPI interface

See chapter SPI Interface Protocol for details.

3. SPI interface protocol

SPI interface has two kinds of command frames. One is read-write command frame used to read and write the register, and the other is convert command frame used to start ADC conversion. If the SCK/PD pin’s signal stays at ‘0’ for more than 100us, then the chip will turn to work mode. If the SCK/PD pin’s signal stays at ‘1’ for more than 100us, then the chip will turn to read/write mode.

3.1. Read-write command frame

The first 8bit of the read-write command frame is shown as follows:

Bit							
7	6	5	4	3	2	1	0
Command							

Bit	名稱	描述
7：0	Command	0xA5：write internal register 0xB5：read internal register

The second 8bit of the read-write command frame is shown as follows:

Bit							
7	6	5	4	3	2	1	0
Data							

Bit	名稱	描述
7：0	Data	Write/read data

The third 8bit of the read-write command frame is shown as follows:

Bit							
7	6	5	4	3	2	1	0
CRC7							

Bit	名稱	描述
7：1	CRC7	CRC checksum, If the CRC7 checksum is failed when writing register, the writing data will be ignored. When reading register data, MCU should check the data by CRC checksum.
0	End Bit，always will be ‘1’	

The following picture is the timing of register write command frame

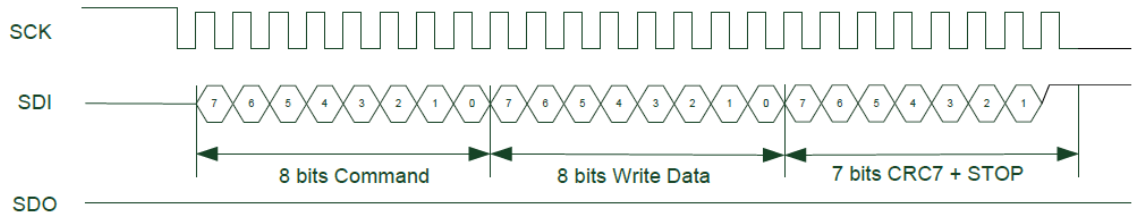


Figure 3-1 **SPI register write command frame**

The following picture is the timing of register read command frame

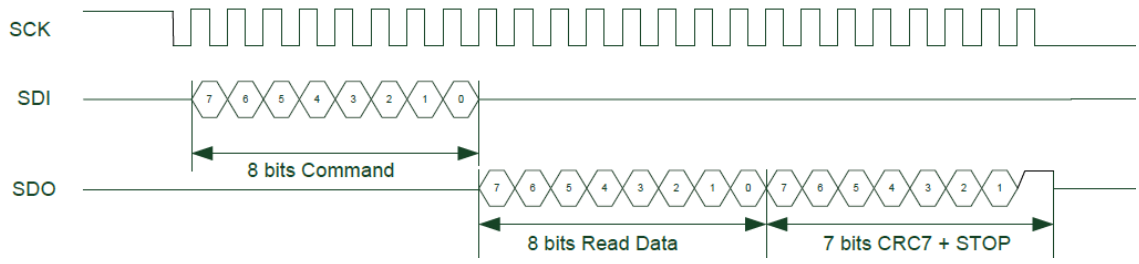


Figure 3-2 **SPI register read command frame**

3.2. Convert command frame

Actually convert mode(or work mode) doesn’ t need SPI command, Set the SCK/PD pin to be ‘0(low)’ for more than 100us, then the chip will turn to work mode. Then MCU could waiting for SDO’ s falling edge to ‘0’ to read the 24bit convert data. When read out the 24 bit data, MCU could send another SCK pulse to make sure the SDO pin turning to high impedance mode. Because there is a 300k Ohm pull up resister from SDO to AVDD, SDO pin will be high when in high impedance mode. The following picture is the timing of converting command frame

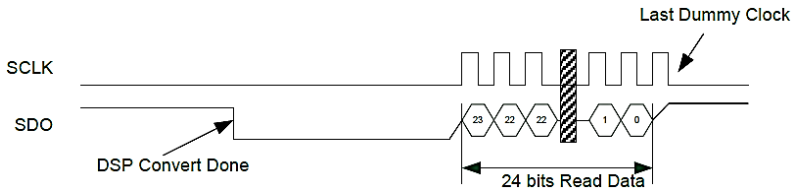


Figure 3-3 SPI timing of converting command frame

3.3. SPI CRC check

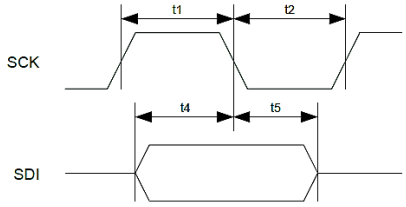
CRC checksum is used to check the correctness of the 8 bit write/read data, the CRC7 is calculated by the following formula: X^7+X^3+1

The following program for CRC7 calculation is for reference.

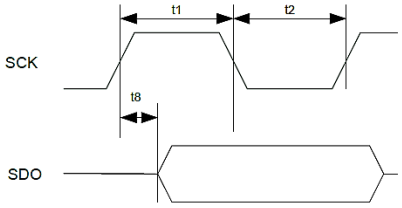
```
shift_reg=data<<24;
crc7=0x5A;
for(i=0;i<8;i=i+1)
   {if((crc7>>6) !=(shift_reg>>31))
    crc7=((crc7<<1)^0x09)&0x7F;
    else
    crc7=(crc7<<1)&0x7F;
    shift_reg<<=1;}
```

For example, when the data is 0xA5, the result of CRC7 check is 0x10.

3.4. Timing of SPI Interface



SPI write timing



SPI read timing

	Identification	Minimum	Typical	Maximum	Unit
SPI timing					
SPI clock frequency	SCLK	0		2	MHz
SPI clock pulse width	t1 (high)	250			ns
	t2 (low)	250			ns
SDI write timing					
Time of DATA ahead of the clock’ s rising edge	t4	50			ns
DATA stable time after clock edge	t5	100			ns
SDI read timing					
Delay time from the SCLK falling edge to new data output	t8			150	ns

When SPI writes data, SDI data change at the SCK’ s rising edge.

When SPI reads data, SDO data change after the SCK’ s rising edge

4. Register description

4.1 Register address

There is one 8-bit registers in XM24LH. The user can choose to read or write by sending the read-write command frame. The following table lists the initial value of the register.

Table4-1 **Register info**

Write Command	Read Command	Register Name	Type	bits	description	Initial value
0xA5	0xB5	ANA_REGIN	R/W	8	Control register	0x00

下面開始針對寄存器做詳細介紹

4.2 ANA_REGIN寄存器 ANA_REGIN register

Table4-2 **ANA_REGIN definition**

Address	Name	Type	Description	Initial value
7：6	DR	R/W	ADC data rate selection 0：10Hz 1：20Hz	0x0
5	BGPEN	R/W	0：use external reference voltage from VREFP pin 1：open internal 1.19V reference voltage module and use this for ADC’ s reference, do not connect to other voltage sources.	0x0
4	SHI	R/W	Short ADC input internally 1：short input	0x0
3	保留	R/W	Reserved. Read as 0. Write as 0.	0x0
2	MODE	R/W	0：Corresponds to the high-power operating mode, with a chip current of 1.5mA when PGA>1. 1：Corresponds to the low-power operating mode, with a chip current of 0.7mA when PGA>1.	0x0
1：0	GA	R/W	ADC Gain setting 0：128 1：64 2：32 3：1	0x0

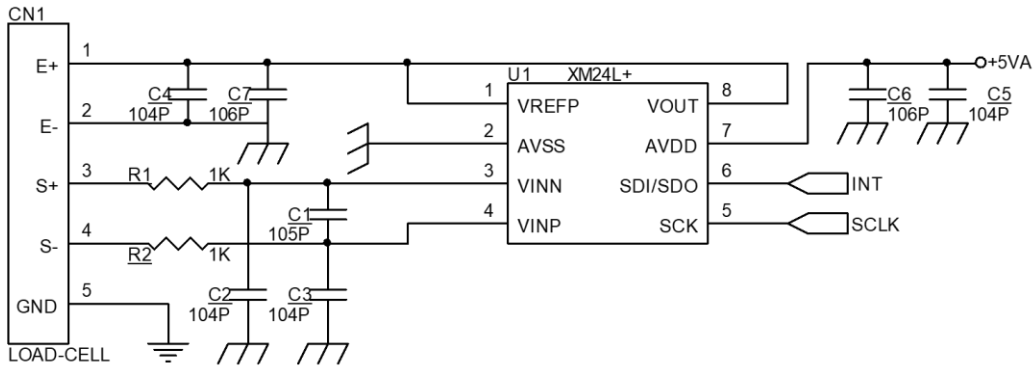
參考例程

```
unsigned long ADvalue;
unsigned char ADi;
/*---------------------------------     CRC7     -----------------------------------*/
unsigned long Crc7(unsigned long REG_data)
{int i;
 unsigned long crc7;
 unsigned long shift_reg;
 shift_reg   = REG_data<<24;
 crc7 = 0x5A;
 for(i=0;i<8;i++)
     {if((crc7>>6)!=(shift_reg>>31)){crc7=((crc7<<1)^0x09)&0x7F;}
       else                                {crc7=(crc7<<1)&0x7F;}
       shift_reg<<=1;}
 return crc7;}
/*--------------------------------     WriteByte     ---------------------------------*/
void Write_One_Byte(unsigned char REG_data)
{unsigned char i;
 for(i=0;i<8;i++)
     {if(REG_data &0x80){AD_SDO_O=1;}
       else                  {AD_SDO_O=0;}
       REG_data<<=1;
       AD_SCLK=1;   delay(0);
       AD_SCLK=0;   delay(0);}}
/*-------------------------------     SPI_WriteByte     -------------------------------*/
void SpiWriteComCheck(unsigned char REG_data) //写命令
{unsigned char crc7;
////////////////////////////////需要注意IO輸出口
 AD_SCLK=0;
 Write_One_Byte(0xA5);
 Write_One_Byte(REG_data);
 crc7=Crc7(REG_data);
 Write_One_Byte((crc7<<1)|0x01);
 AD_SCLK=1; delay(0);}
/*--------------------------------     ADC_SETUP     ---------------------------------*/
void INIT_XM24LP(void)
{AD_SCLK=1; ldelay(200);
SpiWriteComCheck(ANA_REGIN);
 AD_SCLK=0;}
/*--------------------------------     Read_ADC     ---------------------------------*/
void Read_AD_Value(void)
{ ////////////////////////////////需要注意IO是輸入口
 AD_SCLK=0;   ADvalue=0;
 for(ADi=0;ADi<24;ADi++)
     {ADvalue=ADvalue<<1;   AD_SCLK=1; delay(0); AD_SCLK=0; //上升沿接收資料,下降沿更新資料
       if(AD_SDO_I==1&&ADi==0){AD_NEG=1;}
       if(AD_SDO_I==1){ADvalue++;}}
 AD_SCLK=1; AD_SCLK=0;
 ADvalue=ADvalue+0x800000;
 ADvalue=ADvalue&0xFFFFFF;}
```

Application diagrams

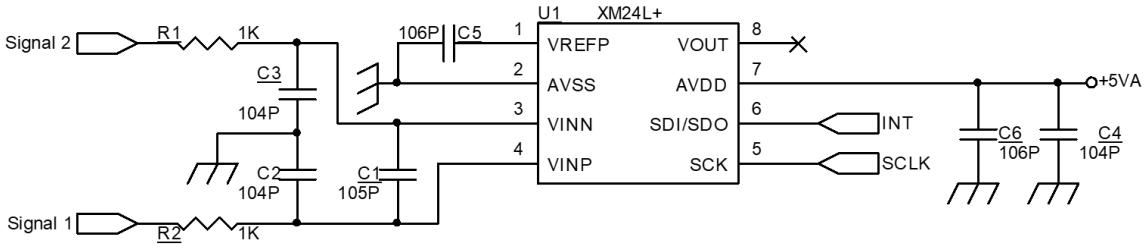
Bridge sensor

- VREFP pin and bridge sensor’ s excitation side is connected to VDD_OUT, when chip is in work mode, the internal switch is turn on to connect VDD_OUT to AVDD. When chip is in sleep mode, the switch is turn off to save power.
- The SDI/SDO pin is multiplexing, so in the MCU side, when SDI is working, the SDO should be set to high impedance mode. when SDO is working, the SDI should be set to high impedance mode.
- The input signal’ s anti-aliasing RC filter in the picture above is just for reference, but the R1/R2’ s value is recommended to be less than 1k Ohm, or else the resistance’ s noise will rising.



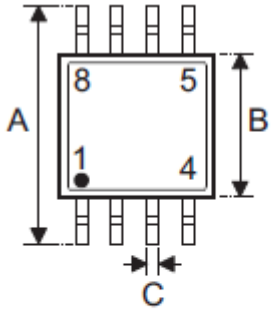
Other sensors

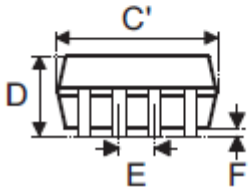
- In some application, the internal 1.19V reference can be used, but this reference can only serve for this chip, the user should not connect the VREFP to other chip or resistance when use internal reference cause the driving capability of internal reference is not so strong to drive others. If VREFP is connected to external voltage sources, the BGPEN bit in register must be set to ‘0’.

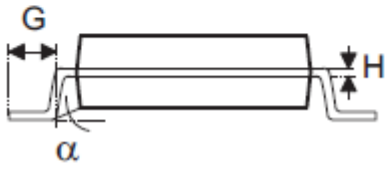


PACKAGING

SOP8







符号	尺寸 (单位：inch)		
	最小值	典型值	最大值
A	—	0.236 BSC	—
B	—	0.154 BSC	—
C	0.012	—	0.020
C′	—	0.193 BSC	—
D	—	—	0.069
E	—	0.050 BSC	—
F	0.004	—	0.010
G	0.016	—	0.050
H	0.004	—	0.010
α	0°	—	8°

符号	尺寸 (单位：mm)		
	最小值	典型值	最大值
A	—	6.00 BSC	—
B	—	3.90 BSC	—
C	0.31	—	0.51
C′	—	4.90 BSC	—
D	—	—	1.75
E	—	1.27 BSC	—
F	0.10	—	0.25
G	0.40	—	1.27
H	0.10	—	0.25
α	0°	—	8°