COOPERATION

24-Bit Sigma-Delta ADC

CS1259

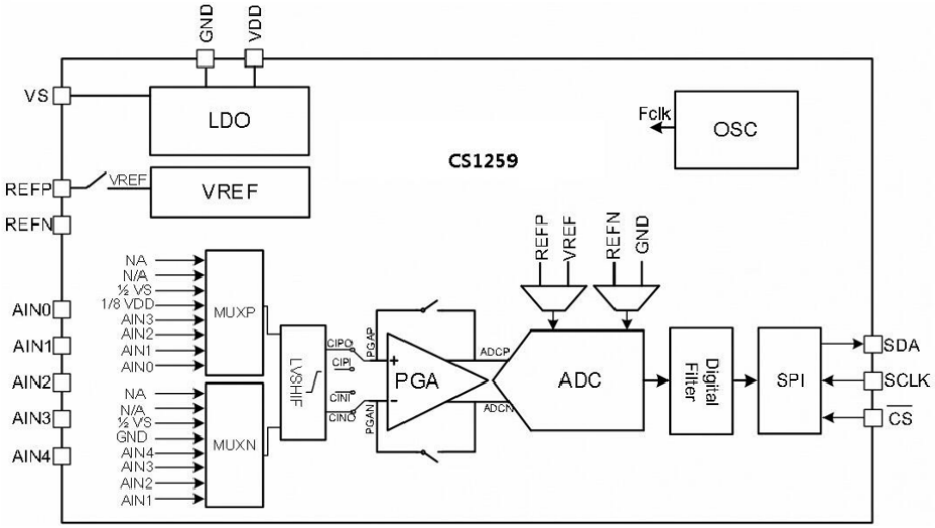
Features

- Supporting single end input；
- Supporting up to 5 inputs combination of multiple differential input pairs；
- Supporting the input voltage level shift function.
- 1/2/4/8/16/32/64/128 times of optional gain；
- Up to 100 MΩ equivalent input impedance.
- 24-bit resolution；
- Optional output rate 10 to 1280 Hz.
- 19.5-bit effective bits under 2.35 V reference, 40 Hz frequency, and 128 times of gain.
- Build-in LDO, 2.35/2.45/2.8/3.0 V optional output.
- Supporting the high-performance, common, low power consumption, and sleep modes；
- Supporting voltage measurement , and single command switching；
- Low drift clock；
- 3-wire serial communication.

Application

- Bridge sensor; Weighing.
- Pressure measurement. Industrial control.
- Chemical analysis.

Functional block



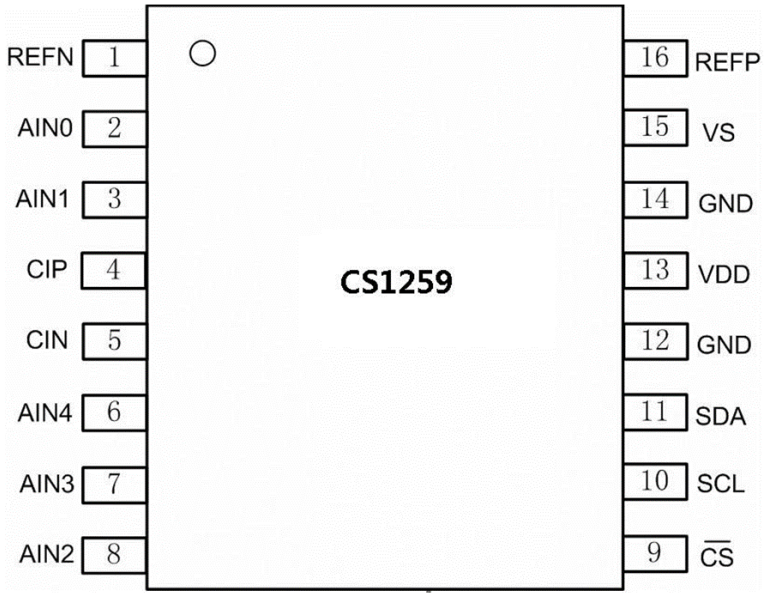
Summary

CS1259 includes an ADC signal chain. The ADC signal chain includes input MUXP/MUXN, a programmable low-noise gain amplifier (PGA), a Sigma-delta ADC, and A digital filter. The MUXP/MUXN has eight input channels, including five external analog input channels and three internal input channels. Behind the MUXP/MUXN, there is a voltage level shift module LVSHIFT, which can shift input signals near ground tracks and transmit them to the PGA. There are multiple gain can be selected by PGA and ADC. The digital filter can be configured with multiple output rates.

CS1259 embeds low drift LDO、voltage reference VREF and high-precision oscillato（OSC）. CS1259 supports configuration of multiple functional modes through the 3-wire serial interface.

For example, CS1259 is used as a bridge sensor and is used for body impedance analysis, and single end input.

Package



SOP16

引脚顺序	引脚名称	类型	说明
1	REFN	I	Negative reference voltage input port
2	AIN0	I	Analog Signal Input Channel 0
3	AIN1	I	Analog Signal Input Channel 1
4	CIP	I/O	Analog signal filter positive port
5	CIN	I/O	Analog signal filter negative port
6	AIN4	I	Analog Signal Input Channel 4
7	AIN3	I	Analog Signal Input Channel 3
8	AIN2	I	Analog Signal Input Channel 2
9	CS	I	Chip Select Signal Port/ Programming Voltage VPP
10	SCLK	I	Serial Communication Clock Port
11	SDA	I/O	Serial Communication Data Port
12	GND	P	Ground
13	VDD	P	Power Source
14	GND	P	Ground
15	VS	O	LDO output port
16	REFP	I	Positive reference voltage input port

Limiting Value

Name	Symbol	Minimum	Maximum	Unit	Description
Supply voltage	VDD	-0.3	6	V	VDD to GND
Instantaneous current of power supply			100	mA	Input Current momentary
Constant current of power supply			10	mA	Input Current continuous
Digital pin input voltage		-0.3	VDD+0.3	V	Digital Output Voltage to GND
Digital output pin voltage		-0.3	VDD+0.3	V	
Junction temperature			150	℃	Max. Junction Temperature
Operating temperature		-40	85	℃	Operating Temperature
Storage temperature		-60	150	℃	Storage Temperature
Chip pin soldering temperature			300	℃	Lead Temperature (Soldering, 10s)

Electrical Characteristics

The whole chip provides the supply voltage from 2.4 V to 3.6 V, with the operating temperature from -40 C to 85 C. The following table lists design specifications.

Test Condition： VDD=3.0V,25℃,VS=2.35V

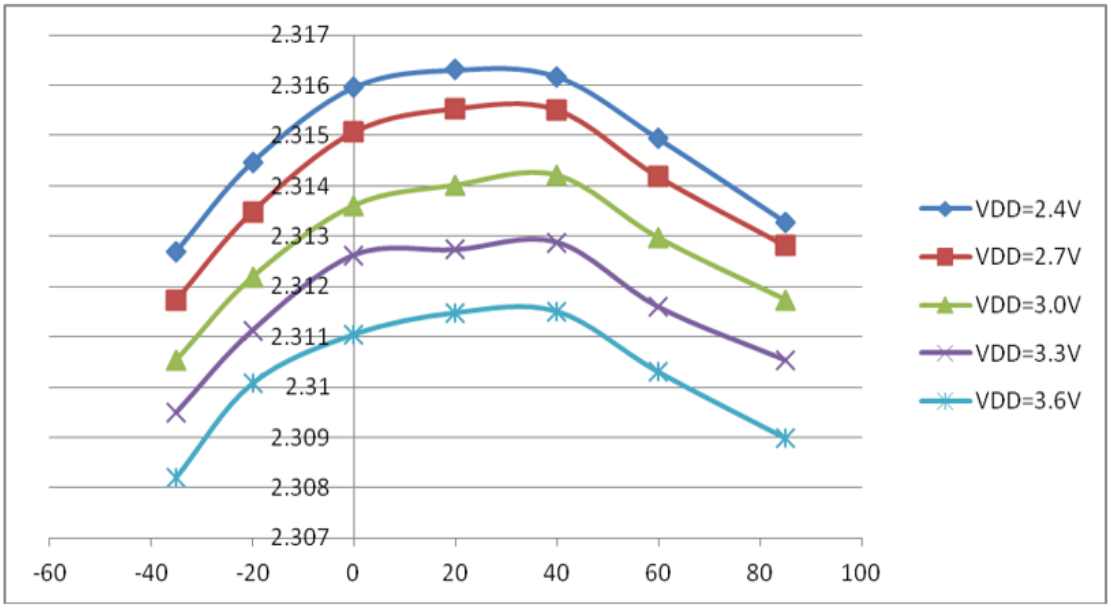
Parameter		Condition	Minimum value	Typical value	Maximu m value	Unit
Analog input	Full amplitude input voltage			±VREF/Gain		V
	Common mode input voltage	PGA Buffer is disabled.	GND-0.1		VS+0.1	V
		PGA Buffer is enabled.	See "PGA and ADC".			
	Differential input impedance	PGA Buffer is disabled.	See "PGA and ADC".			
		PGA Buffer is enabled.		100		MΩ
PGA &ADC	Resolution	No missing code		24		Bits
	Data Rate		10	40	1280	SPS
	Setting time			4		Conversion cycle
	Noise performance	Gain=32×2 160Hz		95		nV
		Gain=1×1, 160Hz		2.3		uV
	Integral linearity	Gain=128		0.0015		% of FS
	Offset error	Gain=128		±8		uV
		Gain=1		±100		uV
	Offset error drift	Gain=128		±0.5		nv/℃
		Gain=1		0.4		uv/℃
	Gain error	Gain=128		±5		%
		Gain=1		±1		%
	Gain error drift	Gain=128		8		ppm/℃
		Gain=1		TBD		ppm/℃
	Input REFP		VS/2		VDD+0.1	
	Input REFN		GND-0.1	GND	VS/2	
LDO &VREF	VS voltage	LDOS[1：0]=00	2.32	2.35	2.38	V
	VS warm-up drift			30		ppm/℃
	VREF voltage		1.212	1.225	1.238	V
	VREF warm-up drift			30		ppm/℃
Clock	frequency			5.898		MHz
	Trim accuracy			1		%
	Total temperature change of frequency			2		%
	Total voltage change of frequency			1		%

Parameter		Condition	Minimum value	Typical value	Maximu m value	Unit
Digital	VIH		0.7×VDD		VDD+0.1	V
	VIL		GND		0.2×VDD	V
	VOH	Ioh=1mA	VDD-0.4		VDD	V
	VOL	IoL=1mA	GND		0.2+GND	V
	IIH	VI=VDD			1	uA
	IIL	VI=GND	-1			uA
	Fsclk				Fosc/4	MHz
Power supply and module power consumption	Supply voltage	VDD	2.4	3	3.6	V
	ADC operating current	Common mode		0.6		mA
		Performance mode		1.1		mA
		Power down		0.1	1	uA
	LDO operating current			160		uA
	VREF operating current	Temperature compensation is enabled.		280		
		Temperature compensation is disabled.		210		uA
	OSC operating current	Freq=5.96MHz		78		uA
	Digital operating current	Normal working		230		uA
		Power down		0.2	1.3	uA
Overall power consumption	ADC+LDO+digital	ADC common mode		1		mA
	ADC+LDO+digital	ADC performance mode		1.5		mA
	ADC+LDO+digital	ADC duty cycle mode		0.4		mA

The preceding noise characteristics indicate the noise characteristics when PMODE[1：0] is 01, BUFBP is 0, and CHOPM[1：0], LVSHIFT, and FIL_EN adopt default configuration.When one or more than one noise characteristic is used, see related description in "Noise and Significant Bit".

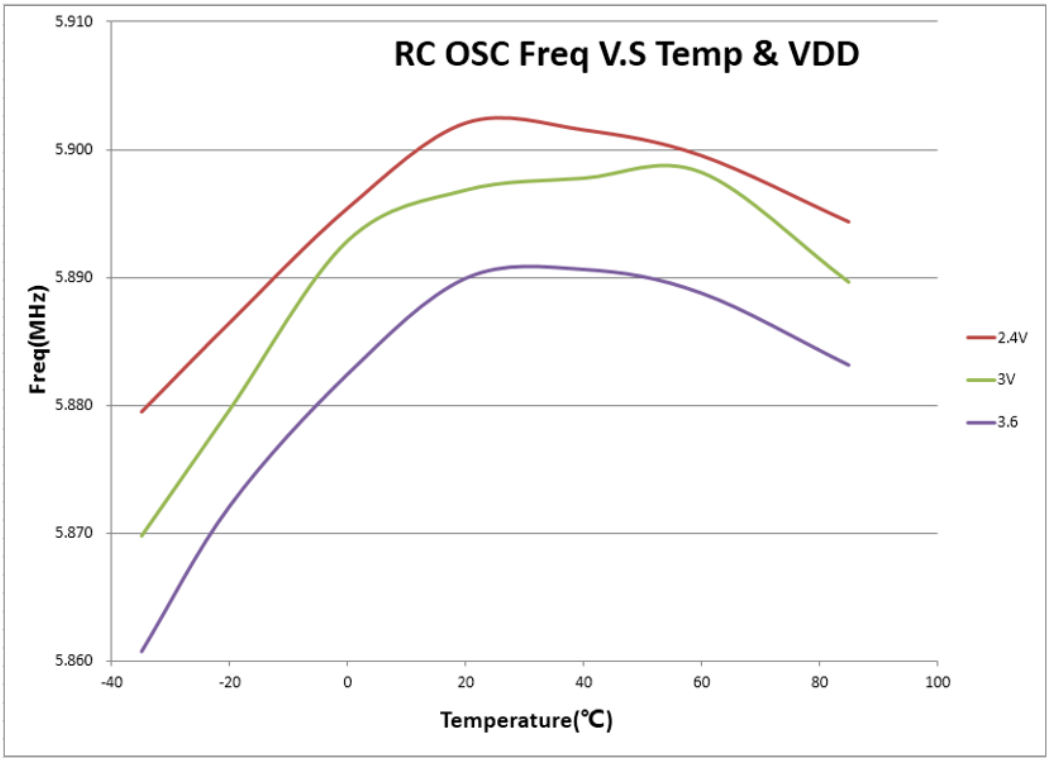
The operating current of LDO and VREF includes the operating current of the internal Bandgap module. Therefore, when the two modules are enabled at the same time, the current is not simple addition. The current of LDO and VREF (temperature compensation is disabled) is 260 uA.

Typical Characteristics of LDO



Typical characteristics of LDO (LDOS[1：0]=00, with 1mA load)

Typical Characteristics of Internal Clock



Typical characteristics in the full voltage and full temperature range of internal clocks

Valid Conversion Bits (ENOB)

Valid bits under different gain and DR for ADC signal chain (ENOB) VDD=3V, VS=2.35V,VIN=±VS/Gain, Tc=25℃, TT

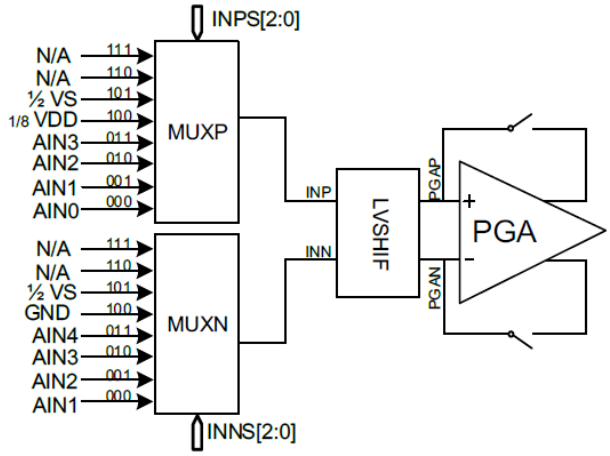
Gain = PGA×ADGN			BUFBP	DR			
				10Hz	40Hz	160Hz	1280Hz
1	1	1	0	22.3	21.2	20.9	18.8
2	1	2	0	21.6	20.6	19.7	18.2
4	1	4	0	21.2	20.3	19.3	17.7
8	1	8	0	20.3	19.7	18.8	17.2
16	16	1	0	22	21.2	20.3	18.7
32	32	1	0	21.4	20.8	19.7	18.3
64	32	2	0	20.8	20	19	17.5
128	32	4	0	20	19.5	18.6	16.9
1	1	1	1	TBD	TBD	TBD	TBD
2	1	2	1	TBD	TBD	TBD	TBD
4	1	4	1	TBD	TBD	TBD	TBD
8	1	8	1	TBD	TBD	TBD	TBD
8	8	1	1	TBD	TBD	TBD	TBD
16	16	1	1	TBD	TBD	TBD	TBD
32	32	1	1	TBD	TBD	TBD	TBD
64	32	2	1	TBD	TBD	TBD	TBD
128	32	4	1	TBD	TBD	TBD	TBD

The preceding noise characteristics are under the following conditions： PMODE[1：0] is set to 01, LVSHIFT is disabled, and FIL_EN is set to 0. The signal source is a bridge resistor, the input common mode voltage is VS/2, the internal resistance is 2Kohm, the common mode capacitance is 100 pF, and the differential filter capacitance is 0.1 uF.

Function Description

Input Selection

The analog input channel and several internal signals of CS1259 pass through MUXP and MUXN respectively, and then connect to the positive and negative terminals of PGA through the level shifting module LVSHIFT as shown in Figure



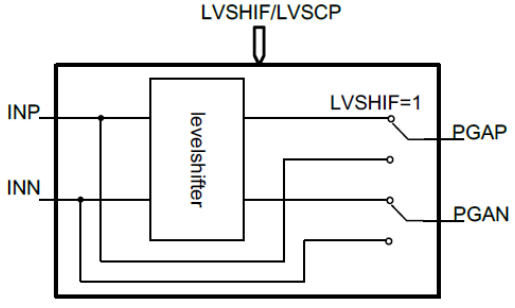
Analog input structure

In the input signal, AINx(x=0 to 4) comes from the corresponding analog input pin and can be combined into a differential pair; REFN is used to pair with AINx to form a single-ended measurement. The REFN pin should be connected to GND (there is no independent REFN in some packages, but REFN is already connected to GND inside the device); 1/8 VDD is paired with REFN to measure the supply voltage; 1/2 VS is used to perform offset calibration.

Input voltage Level Shifter

In some scenarios, when the common mode voltage of the input signal is close to the ground track or the input is the single end signal with one end being grounded, the PGA cannot amplify the signal. The input voltage level shift module can raise the common mode voltage of the signal close to the ground track by about 0.9 V so that the signal can be properly amplified by the PGA.

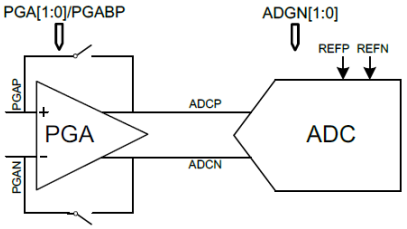
As shown in Figure , when LVSHIFT is 1, INP and INN pass the level shifter and are output to the PGAP and PGAN. On the contrary, INP and INN directly pass the PGAP and PGAN. The LVSCP control bit is the chopping control bit. After chopping is enabled, the offset brought by the level shifter and low-frequency noise are reduced.



Level shift module

PGA and ADC

CS1259 amplifies the input signal through a low-noise and low-drift PGA and transmits the signal to a second-order Sigma-Delta ADC for analog-to-digital conversion. Figure shows the structures of the PGA and ADC. The gain of the PGA is selected through PGA[1：0] and the options are 1, 8, 16, and
32. The gain of the ADC is selected through ADGN[1：0] and the options are 1, 2, 4, and 8. In addition, reference voltage is from the input REFP-REFN.



Structures of the PGA and ADC

T he gain of the input signal is determined by the product of the gain of the PGA and ADC.

$$Gain = PGA \times ADGN \quad \text{(Formula 1)}$$

To improve the signal setup performance, there is a Buffer between the PGA output and the input of the ADC modulator. In addition, the buffer bypass function is provided. If BUFBP is set to '1', the buffer is bypassed and the signal output by the PGA is directly connected to the modulator of the ADC. The differential full_scale input voltage range FS of CS1259 is determined by the gain.

$$FS = (REFP - REFN) / Gain \quad \text{(Formula 2)}$$

If the differential input channel AINp-AINn=VIN, the range of VIN must be smaller than FS to ensure that overflow does not occur. When the PGA is enabled (including scenario PGA≠1 and PGA=1&BUFBP=0), the input signal range of the input channel must ensure that the PGA can work properly and is generally as follows：

$$VDD - 1.0V > AINx > GND + 0.2V \quad \text{(Formula 3)}$$

The common mode voltage of the input signal is VCM. If VCM = (AINp + AINn)/2, the VCM range is determined by the PGA

$$VDD - 1.0V - VIN \times PGA/2 > VCM > GND + 0.2V + VIN \times PGA/2 \quad \text{(Formula 4)}$$

When PGA is 1 and BUFBP is 1, the PGA is bypassed. In this case, the input signal directly connects the ADC and the input signal range is determined by the ADC. Generally：

$$VDD + 0.1V > AINx > GND - 0.1V \quad \text{(Formula 5)}$$

The VCM range is also determined by the ADC.

$$VDD + 0.1V - VIN \times ADGN/2 > VCM > GND - 0.1V + VIN \times ADGN/2 \quad \text{(Formula 6)}$$

The preceding circumstances also affect the equivalent input impedance of input channels. For details, see Table

Relationship between gain and input signal for the PGA and ADGN

Gain = PGA × ADGN			BUFBP	Input impedance	Input signal range	Common mode input range
1	1	1	0	>100Mohm	(Formula 3)	(Formula 4)
2	1	2	0			
4	1	4	0			
8	1	8	0			
16	16	1	0			
32	32	1	0			
64	32	2	0			
128	32	4	0			
1	1	1	1	~800Kohm	(Formula 5)	(Formula 6)
2	1	2	1	~400Kohm		
4	1	4	1	~200Kohm		
8	1	8	1	~100Kohm		
16	16	1	1	>100Mohm	(Formula 3)	(Formula 4)
32	32	1	1			
64	32	2	1			
128	32	4	1			

When the input signal is close to the ground track, for example, single end signal, and you hope to enable the PGA to obtain higher gain and input impedance, you can enable the LVSHIFT function, shift up the input signal by about 0.9 V, and transmit the signal to the PGA. This is equivalent to the following circumstance： After the LVSHIFT function is enabled, the PGA is enabled and the lower limit of the input signal is shifted down by around 0.9 V.

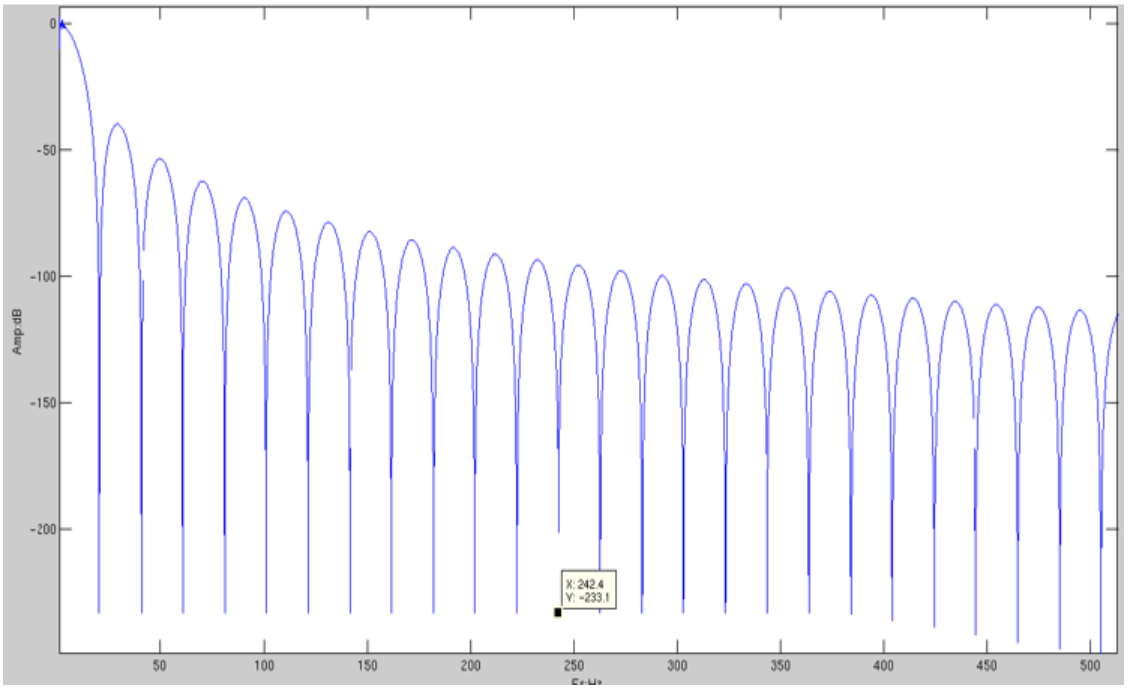
The ADC of CS1259 adopts a second-order sigma-delta modulator to implement voltage regulation. When the internal sampling frequency is 331.11 kHz (common mode) or 662.22 kHz (high- performance mode), the gain ADGN can be implemented through multiplication of the capacitance and frequency.

The ADC of CS1259 provides the internal gain temperature drift compensation, which can be configured through GTCSL and GTC[2 : 0]. When GTCSL is 1, coarse adjustment is provided. In this case, a step of GTC[2 : 0] gain temperature drift compensation is 30 ppm/ C and the function can be used to compensate temperature drift of an external sensor; when GTCSL is 0, the corresponding step is 5 ppm/ C and the function can be used to compensate gain temperature drift inside the chip.

Digital Filter

Data from the Sigma-delta ADC is 1-bit high-speed bit stream data and includes lots of high- frequency noise. Therefore, a digital filter needs to be used to filter bit stream data and convert the bit rate so as to filter out high-frequency noise, complete down-sampling, and convert 1-bit high-speed bit stream data into 24-bit second-phase binary data. The operation is completed through a multi-order COMB filter. In addition to the COMB filter, you can choose whether to use a filter for further filtering

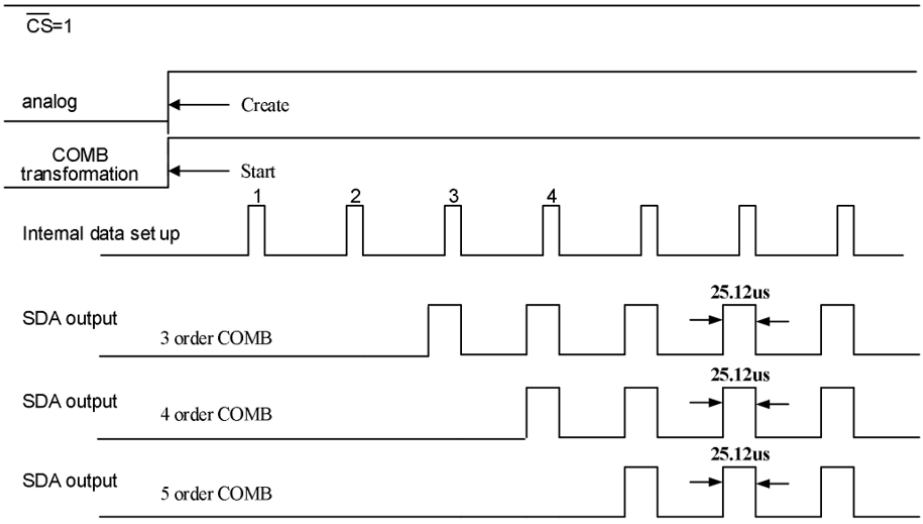
Frequency Response



Frequency response characteristics of the COMB filter (Fs=331 Hz, DR=10Hz, three-order COMB)

Setting Time

In normal mode, the COMB filter works at a low speed in the third-order (10 Hz, 20 Hz, 40 Hz, and 80 Hz) or works at a high speed in the fourth-order or fifth-order (160 Hz, 320 Hz, 640 Hz, and 1280 Hz). In duty cycle mode, a digital COMB filter works in the fourth-order or fifth-order. The data setting time is related to the COMB order. Data of a third-order COMB filter can be created in the third order; data of a fourth-order COMB filter can be created in the fourth order; data of a fifth-order COMB filter can be created in the fifth order.



COMB creation process

If FIL_EN is set to 1, the data creation time is longer. The following table lists the required time (the data error is converged to the time with less than 1/10000)

FILCON1	FILCON0	Creation time
0	0	COMB data creation time +300ms
0	1	COMB data creation time +590ms
1	0	COMB data creation time +230ms
1	1	COMB data creation time +460ms

Reference Voltage Source

CS1259 integrates a low-drift LDO, which can output voltage to VS and/or REFP. The options are 2.4 V, 2.6 V, 2.8 V, and 3.0 V and are provided to VS. The LDO is used to supply power to external bridge sensors and internal ADC. The maximum current of load is 10 mA. The chip also includes an internal reference voltage source VREF whose output is 1.225 V. It is used as reference voltage of measurement and is provided to REFP (an external capacitor is connected to improve precision) or is used as internal reference voltage VREF. The initial precision of output voltage of the reference voltage source is ±1% and the typical temperature drift coefficient is 30 ppm/ C (-40 to 85℃)。

Internal Clock Source

CS1259 provides a low-drift RC clock inside. The clock frequency is 5.898 MHz. In the range from -40 to 85 C, drift is smaller than 2%; in the VDD voltage range 2.4 to 3.6V, the change is smaller than 1%.

Measurement Mode and Switching

In addition to 5 external analog signal input channels, CS1259 has internal analog signal channels, including supply voltage signal. By configuring the TMODE[1：0] register, you can switch among supply voltage measurement and manual measurement mode. For the first modes, the channel, gain, and output rate are configured internally in advance. In manual mode, you can set related parameters. In manual mode, when you switch to any other mode and switch back to the manual mode, the settings remain unchanged.

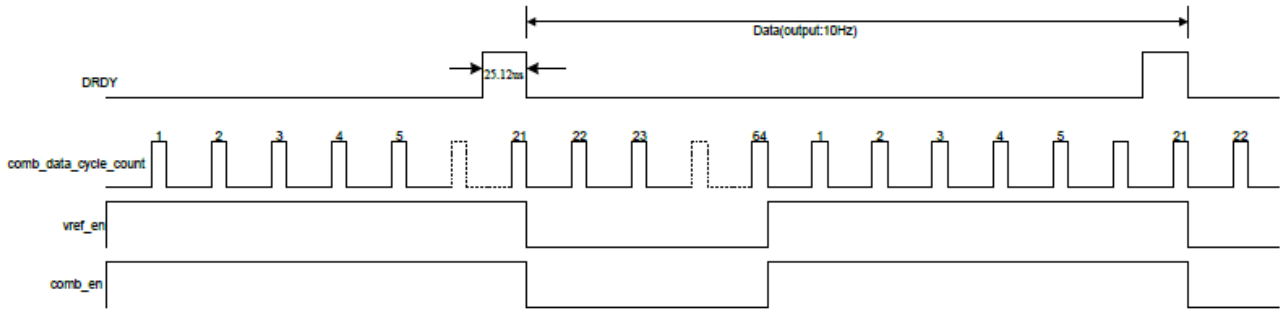
Operating Mode

CS1259 provides multiple operating modes for your choice, including high-performance mode, normal mode, and low power consumption mode. In high-performance mode, the buffer in the PGA is enabled and the sampling frequency of the modulator in the ADC is 662.22 KHz. In this case, the signal precision of the ADC is the highest and the gain temperature

drift and linear performance is the best. In addition, the power consumption of the ADC signal chain reaches 1.5 mA. The high-performance mode can be used in the measurement scenarios requiring 10 Hz SPS and scale division of more than 10000 points. The normal mode balances the power consumption and performance. The buffer is bypassed and the sampling frequency is reduced to 331.11 kHz. The normal mode can be used in scenarios requiring the scale division of less than 10000 points (for example, human body weighing). The power consumption of the ADC signal chain is 1.2 mA. The low power consumption mode achieves power consumption by using duty cycle. In a cycle of 10 Hz data update frequency, a digital filter works at the output rate of 640 Hz. After the ADC is enabled, the first five pieces of data are discarded and data of corresponding quantity is accumulated for averaging. In duty cycle mode, the VREF output and digital circuit work in an intermittent way to reduce power consumption of the chip.

In duty cycle mode, COMB works in the fourth order at a high speed. The data output rate of SPI is only 10 Hz.

The data output rate of COMB is 640 Hz. In 64 COMB cycles, SPI outputs only one piece of data. We can make COMB output only the first 21 pieces of data (the first 5 pieces of data of COMB are lost and the accumulated 16 (16 to 21) pieces of data for averaging are output). For later 43 pieces of data, periodically disable COMB and VREF output. The following figure shows the schematic diagram.



Schematic diagram of CS1259 in low power consumption mode

Note： The data output rate and accumulated data quantity of COMB are configurable

POR and Power down)

When the chip is powered on, the built-in power-on reset circuit generates a reset signal to make the chip reset automatically.

When SCLK works from low level to high level and maintains at high level for 172 μs, CS1259 enters the PowerDown mode. When the SCLK restores to low voltage level, the chip recovers to the normal operating status.

When the system enters the normal operating mode from PowerDown, all functions are configured in the state before PowerDown and functions do not need to be configured.

Description of Functional Registers

List of Functional Registers

Register		Bit								Default value
Address	Name	BIT7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0	
00H	SYS	TMODE[1：0]		PMODE[1：0]		ENREF	ENADC	ENLDO		00H
01H	ADC0	IMOD	FS_SEL	INNS[2：0]			INPS[2：0]			00H
02H	ADC1	DR[2：0]			BUFBP	PGA[1：0]		ADGN[1：0]		00H
03H	ADC2									00H
04H	ADC3	GTCSL	GTC[2：0]			LVSCP	LVSHIFT			00H
05H	ADC4	CHOPM[1：0]		ACCU_NUM[1：0]		ADREFS[1：0]		LDOS[1：0]		40H
06H	ADC5				EXFIL_EN		FIL_EN	FIL_CON1	FIL_CON0	00H
09H	ADOH	ADO[23：16]								00H
	ADOM	ADO[15：8]								00H
	ADOL	ADO[7：0]								00H
0AH	ADS	ADS	RST							00H

Description of Functional Registers

SYS — System Configuration Register (Address 00H)

Bits	Description		Permission	Default value
[7：6]	TMODE[7：6]	**Measurement mode control bit** 11： NA 10： supply voltage measurement mode (Set ENREF to 1, INPS[2：0] to 100, INNS[2：0] to 100, LVSHIFT to 0, PGA[1：0] to 00, BUFBP to 0, ADGN[1：0] to 00, ADREFS[1：0]=10,FS_SEL to 0, and IMOD to 0 and set corresponding registers to invalid registers. Others are determined by registers.) 01： NA 00： manual measurement mode (Free configuration)	r/w	00′ b
[5：4]	PMODE[1：0]	**Working mode control bit (valid only when TMODE is set to 00)** 11： free mode (ADC free configuration) 10： duty cycle mode, DR=640Hz (FS_SEL is 0, BUFBP is 0, IMOD is 0, and ENADC and ENLDO are controlled.) 01： high-performance mode (Set FS_SEL to 1, BUFBP to 0, and IMOD to 1 and set corresponding registers to invalid registers. Other configurations are determined by corresponding registers.) 00： common mode (currently unavailable) (Set FS_SEL to 0, BUFBP to 1, and IMOD to 0 and set corresponding registers to invalid registers. Other configurations are determined by corresponding registers.)	r/w	00′ b
[3]	ENREF	**VREF module enable signal** 1： Enable VREF. 0： Disable VREF.	r/w	0′ b
[2]	ENADC	**ADC module enable bit** 1： Enable the ADC. 0： Disable the ADC.	r/w	0′ b
[1]	ENLDO	**LDO module enable bit** 1： Enable LDO. 0： Disable LDO.	r/w	0′ b
[0]	NA		r/w	0′ b

ADC0 — ADC Configuration Register (Address 01H)

Bits	Description		Permission	Default value
[7]	IMOD	**Modulator MOD current control bit** 1： current in high-performance mode = current in common mode x 2 0： current in common mode	r/w	0′ b
[6]	FS_SEL	**Sampling frequency selection bit** 1： 662.22 kHz 0： 331.11 kHz	r/w	0′ b
[5：3]	INNS[2：0]	**PGA negative port input signal selection bit** 111： N/A 110： N/A 101： 1/2 VS (common mode voltage) 100： GND (valid only when TMODE is set to 10) 011~000： AIN4~AIN1	r/w	000′ b
[2：0]	INPS[2：0]	**PGA positive port input signal selection bit** 111： N/A 110： N/A 101： 1/2 VS (common mode voltage) 100： 1/8 VDD (valid only when TMODE is set to 10) 011~000： AIN3~AIN0	r/w	000′ b

ADC1 — ADC Configuration Register 1 (Address 02H)

Bits	Description		Permission	Default value
[7：5]	DR[2：0]	**ADC input rate selection bit** 111： 1280Hz 110： 640Hz 101： 320Hz 100： 160Hz 011： 80Hz 010： 40Hz 001： 20Hz 000： 10Hz	r/w	000′ b
[4]	BUFBP	**Buffer control bit** 1： Disable the buffer (currently unavailable). 0： Enable the buffer.	r/w	0′ b
[3：2]	PGA[1：0]	**PGA gain selection bit** 11： Gain = 32 10： Gain = 16 01： Gain = 1 00： Gain = 1	r/w	00′ b
[1：0]	ADGN[1：0]	**Modulator gain selection bit** 11： Gain = 8 (DR goes to 1/4) 10： Gain = 4 (DR goes to 1/2) 01： Gain = 2 00： Gain = 1	r/w	00′ b

ADC2 — ADC Configuration Register 2 (Address 03H)

Bits	Description		Permission	Default value
[7：0]	N/A		r/w	00H

ADC3 — ADC Configuration Register 3 (Address 04H)

Bits	Description		Permission	Default value
[7]	GTCSL	**Gain warm-up drift compensation thickness selection bit** 1： coarse adjustment = fine adjustment x 6, used to compensate warm-up drift of the sensor. 0： fine adjustment, used to adjust warm-up drift of the chip.	r/w	0′ b
[6：4]	GTC[2：0]	**Gain warm-up drift compensation selection bit (CTCSL=0)：** 111： 15 ppm/ C 110： 10 ppm/ C 101： 5 ppm/ C 100： 0 000： 0 001： -5 ppm/ C 010： -10 ppm/ C 011： -15 ppm/ C	r/w	000′ b
[3]	LVSCP	**Level shift module chopping enable bit (valid when LVSHIFT is set to 1)：** 1： Enable chopping. Chopping frequency = Fs/128 0： Disable chopping.	r/w	0′ b
[2]	LVSHIFT	**Level shift module enable bit：** 1： Enable level shift. 0： Disable level shift.	r/w	0′ b
[1：0]	N/A		r/w	00′ b

ADC4 — ADC Configuration Register 4 (Address 05H)

[7：6]	CHOPM[1：0]	**仪放(IA)及调制器(MOD)斩波频率控制位** **Instrument amplifier (IA) and modulator (MOD) chopping frequency control bit** 11： The chopping frequency of the IA is fs_clk/64 and the chopping frequency of the modulator is fs_clk/128. 10： The chopping frequency of the IA is fs_clk/32 and the chopping frequency of the modulator is fs_clk/128. 01： The chopping frequency of the IA is fs_clk/32 and the chopping frequency of the modulator is fs_clk/256. 00： Disable chopping. Fs_clk indicates the sampling frequency of MOD	r/w	01′ b
[5：4]	ACCU_NUM [1：0]	**COMB data cumulative number selection in duty cycle mode** ACCU_NUM / Cumulative number 00 / 8 01 / 16 10 / 32 11 / 64 Note： The result of (COMB data cumulative number + 4) * ADC output rate cannot be greater than the COMB rate 640 Hz.	r/w	00′ b

Bits	Description		Permission	Default value
[3：2]	ADREFS[1：0]	**ADC reference voltage selection bit** 11： positive reference = internal VREF; negative reference = GND 10： positive reference = internal VREF; negative reference = GND 01： positive reference = VREF, which is external connected to REFP, then it links back to ADC. Negative reference = external REFN 00： positive reference = external REFP; negative reference = external REFN	r/w	00′ b
[1：0]	LDOS [1：0]	**Internal LDO output VS voltage selection bit** 11：3.0V 10：2.8V 01：2.45V 00：2.35V	r/w	00′ b

ADC5 — ADC Configuration Register 5 (Address 06H)

Bits	Description		Permission	Default value
[7：5]	NA	NA		
[4]	EXFIL_EN	**Enable bit for PGA input signal to connect an external filter** 1： Use an external RC filter. 0： Not use an external RC filter.	r/w	0′ b
[3]	REG_NC	**Reserved bit**		
[2]	FIL_EN	**Low-pass filter enable control signal after COMB** 1： Enable the filter. 0： Disable the filter. Note： The bit is unavailable in duty cycle mode and cannot be used when the rate is 10Hz, 20Hz, 40Hz, or 80Hz.	r/w	0′ b
[1]	FIL_CON1	**Filtering cascading control** 0： The filter uses the cascade structure. 1： The filter does not use the cascade structure.	r/w	0′ b
[0]	FIL_CON2	**Filter coefficient control** 0： Use coefficient 1. 1： Use coefficient 2.	r/w	0′ b

ADO — ADC Conversion Data Register (Address 09H)

Bits	Description		Permission	Default value
ADOH[7：0]	ADO[23：16]	[23：16] bit of ADC conversion value	r	00H
ADOM[7：0]	ADO[15：8]	[15：8] bit of ADC conversion value	r	00H
ADOL[7：0]	ADO[7：0]	[7：0] bit of ADC conversion value	r	00H

ADS — ADC Conversion Data Read Standard Register (Address 0AH)

Bits	Description		Permission	Default value
[7]	ADS	**ADO data read flag** 1： Data is read. 0： Data is not read.	r	0′ b
[6]	RST	**Chip power-on reset flag bit** 1： Chip power-on reset is complete. 0： This bit is automatically reset after the user queries the flag.	r	0′ b
[5：0]	NA			000000′ b

3-Wire Serial Communication Interface

CS1259 adopts 3-wire serial communication, where CS indicates the chip-select or reset signal, SCLK indicates the communication clock, SDA is the bidirectional data line and the data conversion completion flag.

CS： Serial interface chip-select signal, which is valid under low voltage level. The input signal is internally suspended. You are advised to connect a pull-up resistor.

When the voltage level of CS becomes low from high, it indicates the current chip is selected and i s in the communication status. When the voltage level of CS becomes high from low, it indicates communication ends and the communication interface is reset and in the idle state.

SCLK： Serial clock input pin, which determines the transmission rate on the SPI port. All data transmission operations are synchronous with SCLK. Data is output from the SDA pin on the scl rising edge and read on the SDA on the scl falling edge.

SDA： Serial data input/output pin. When CS is 1, the SDA outputs DRDY, indicating that ADC conversion data is ready; when CS is 0, it indicates the SDA serial communication data port.

The serial communication command register is an 8-bit register. For the read and write operation, bit 7 of the command register is used to determine whether the current data transmission operation type is read operation or write operation. Bits 6 to 0 of the command register indicate the address of the register. For special command operations, bits 7 to 0 are permanently 0xEA.

Note： When SCLK maintains low level around 687 us, the system enters the communication reset mode (only the serial communication interface is reset to prevent the communication interface from becoming abnormal and to prevent communication failure).

Command name	Command register	Data	Description
Read command	{0,REG_ADR[6：0]}	Read_Data	Data is read from the register whose address is REG_ADR[6：0]. Note： If an invalid address is read, the returned value is 00h.
Write command	{1,REG_ADR[6：0]}	Write_Data	Data is written to the register whose address is REG_ADR[6：0].
Reset command	0xEA	0x96	Reset instruction. After the instruction is received, the chip is reset.

Read Time Sequence

Working process：

After CS become valid, an external device first writes the read command bytes through SDA. After CS1259 receives the command, CS1259 outputs the data by bit at the rising edge of SCLK from the SDA pin. Note：

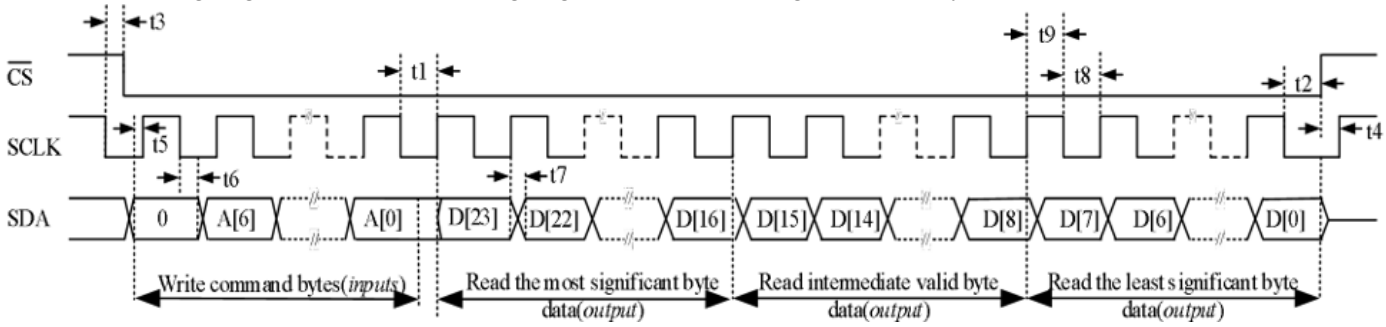
Data is transmitted in the unit of byte. High bits precede over low bits.

For a multi-byte register, high-byte content is first output and then low-byte content is transmitted.

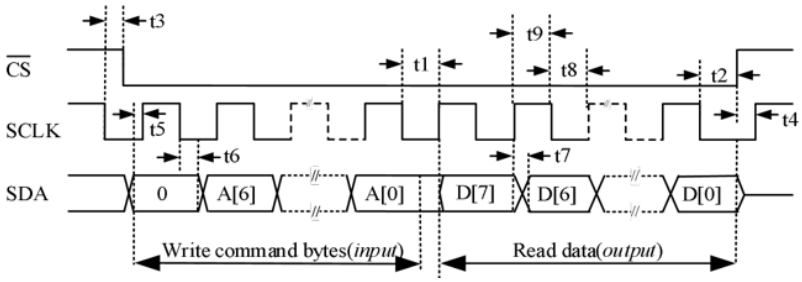
An external device writes command bytes at the rising edge of SCLK. CS1259 outputs the data at the rising edge of SCLK from the SDA.

The time t1 between data bytes must be longer than two system clock periods.

After the LSB of the last byte is transmitted, the level of CS becomes high and data transmission is complete. The time t2 between the falling edge of SCLK and the rising edge of CS must be longer than two system clock periods.



Time sequence of the read operation 1 (the AD value is read)



Time sequence of the read operation 2 (registers except the AD value)

Write Time Sequence

Working process：

After CS becomes valid, an external device first writes command bytes through SDA and then writes data bytes. Note：

1) Data is transmitted in the unit of byte. High bits precede over low bits.

2) For a multi-byte register, high-byte content is first transmitted and then low-byte content is transmitted.

3) An external device writes data at the rising edge of SCLK. CS1259 reads data at the falling edge of SCLK.

4) The time t1 between data bytes must be longer than two system clock periods.

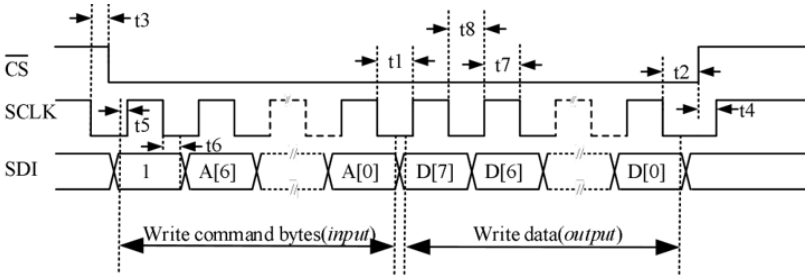
5) After the LSB of the last byte is transmitted, the level of CS becomes high and data transmission is complete. The time t2 between the falling edge of SCLK and the rising edge of CS must be longer than two system clock periods.

Note： For registers supporting the write protection function, the enable command must be written before the write operation is performed.

6) The time t1 between data bytes must be longer than two system clock periods.

7) After the LSB of the last byte is transmitted, the level of CS becomes high and data transmission is complete. The time t2 between the falling edge of SCLK and the rising edge of CS must be longer than two system clock periods.

Note： For registers supporting the write protection function, the enable command must be written before the write operation is performed.



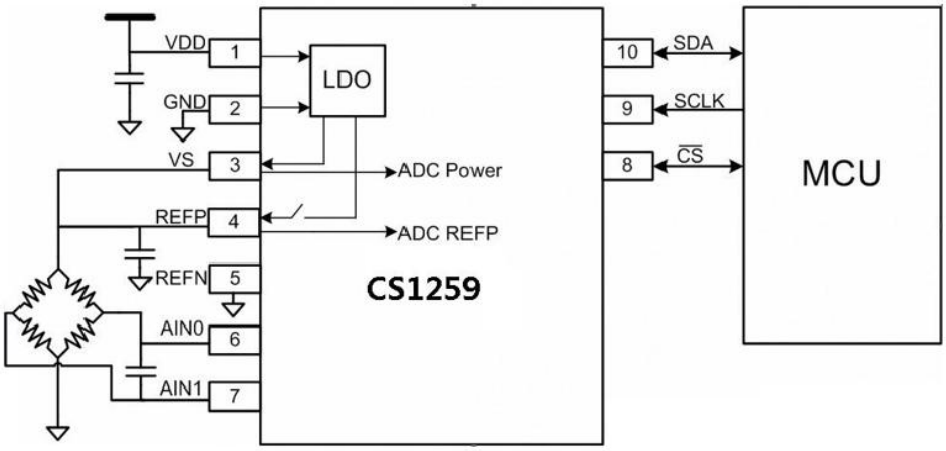
Time sequence of the write operation

Time sequence of the 3-cable serial communication interface

VDD=3V, GND=0V, Fosc=5.898MHz,常温

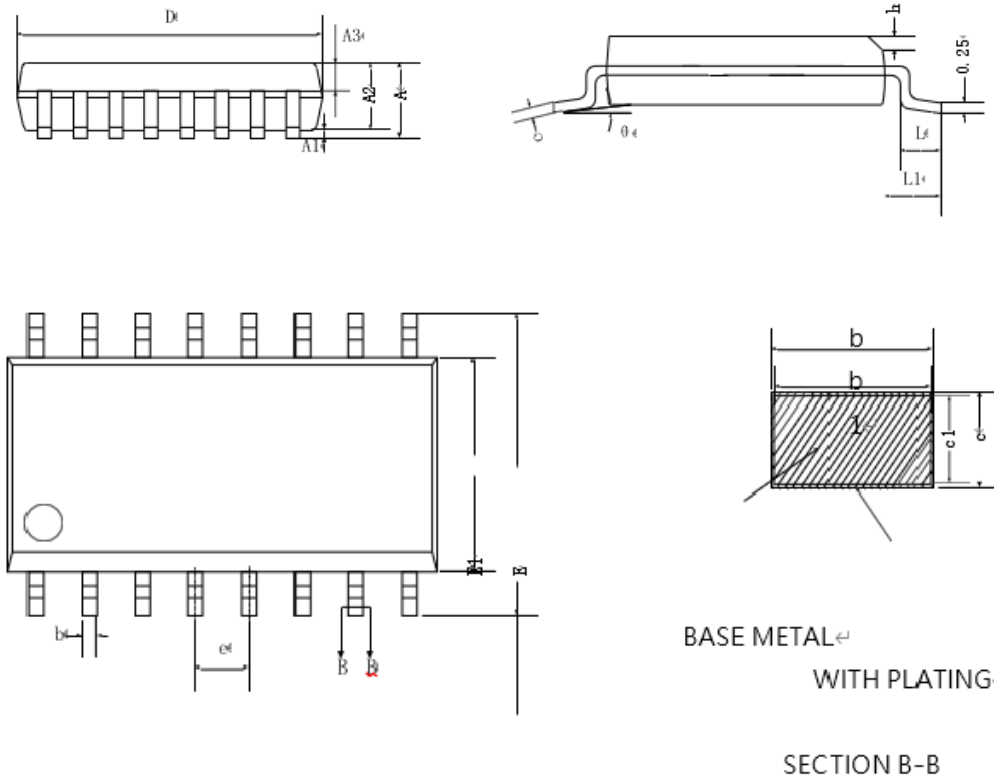
Name	Description	Min	Typ	Max	Unit
t1	Duration in which SCLK maintains low level between data bytes	2*sysclk	-	-	ns
t2	Interval between the last falling edge of SCLK and the rising edge of CS	2*sysclk	-	-	ns
t3	Duration in which SCLK maintains low level before the falling edge of CS	5	-	-	ns
t4	Duration in which SCLK maintains low level after the rising edge of CS	5	-	-	ns
t5	Time in which valid data is created on SDA before the rising edge of SCLK	5	-	-	ns
t6	Time in which valid data is maintained on SDA after the falling edge of SCLK	sysclk	-	-	ns
t7	Time required for SDO to provide stable output after the rising edge of SCLK	50	-	-	ns
t8	High level width of SCLK	2*sysclk	-	170	us
t9	Low level width of SCLK	2*sysclk	-	680	us

Typical Application Circuit



PACKAGING

16-pin SOP 外形尺寸



SYMBOL	MILLIMETER		
SOP16L	MIN	NOM	MAX
A			1.75
A1	0.05		0.225
A2	1.30	1.40	1.50
A3	0.60	0.65	0.70
b	0.39		0.48
b1	0.38	0.41	0.43
c	0.21		0.26
c1	0.19	0.20	0.21
D	9.70	9.90	10.10
E	5.80	6.00	6.20
E1	3.70	3.90	4.10
e	1.27BSC		
h	0.25		0.50
L	0.50		0.80
L1	1.05BSC		
θ	0		8°