DATA SHEET

LCD MODULE

MODULE NO. :

TGG12864-68 SERIES

Customer:
Approved by:

Sonytek Display Co., Ltd.		
Approved by	Checked by	Prepared by

RECORDS OF REVISION

Part Number	Revision	Revision Content	Revised on
TGG12864-68	00	First issue	June. 24th, 2015
TGG12864-68	01	Update Page 4,5,6,8 and 18	July. 14th, 2015
TGG12864-68B	02	Add 68B	Oct. 08th, 2016

CONTENTS

1. FUNCTIONS & FEATURES

- TGG12864-68 Series LCD type:

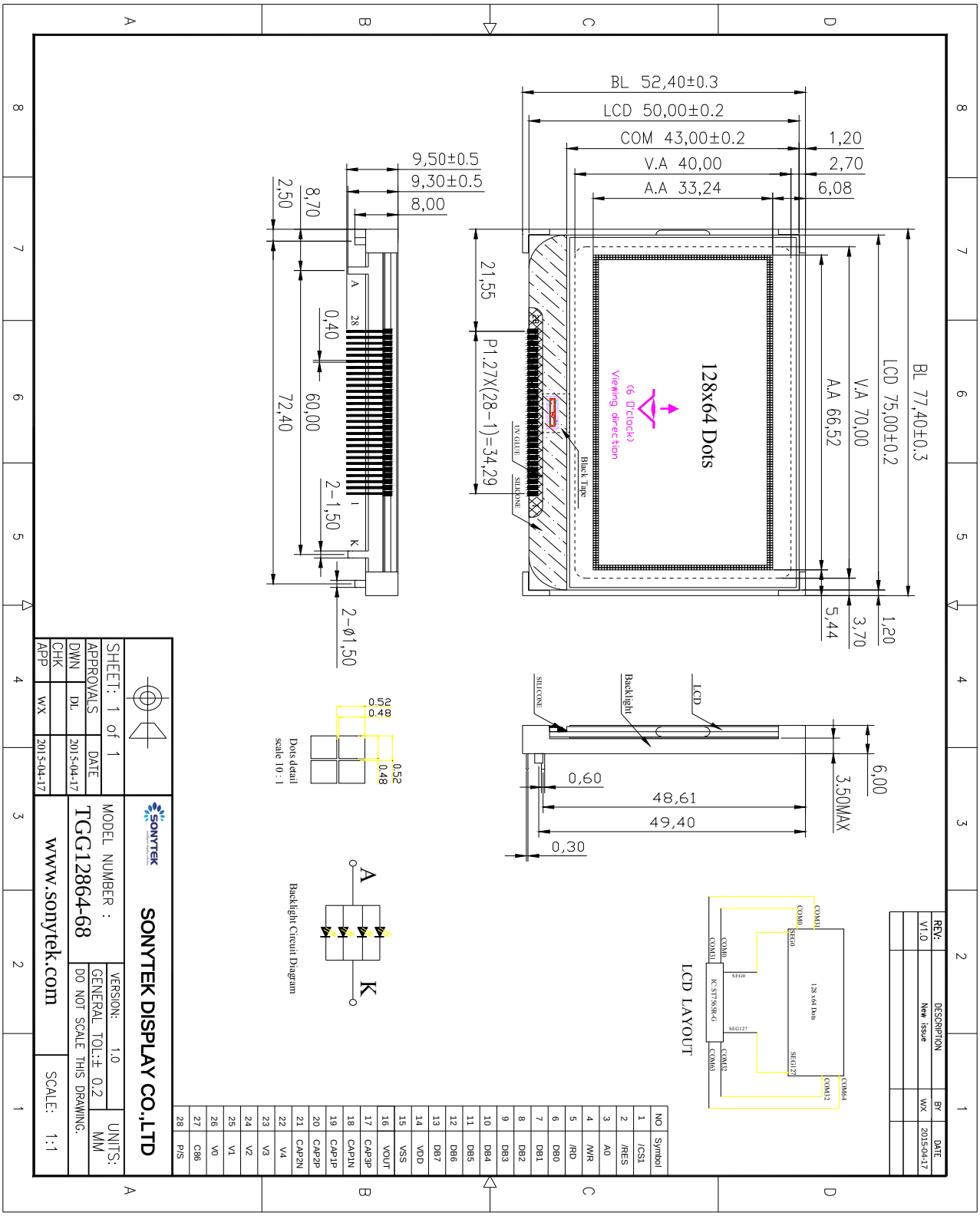
Module	LCD Type	Remark
TGG12864-68A	FSTN Transflective Positive Mode	
TGG12864-68B	STN-Blue Transimmive Negative Mode	

- Display Contents : 128 x 64 Dots
- Driving Scheme : 1/65Duty; 1/9Bias
- Viewing Direction : 6 O' clock
- Power Supply Voltage : 3.0V.
- Driver IC : ST7565R-G
- Interface : Parallel & SPI
- Backlight :White
- Operating Temperature :-20℃ — + 70℃
- Storage Temperature :-30℃ — + 80℃
- RoHS Compliant

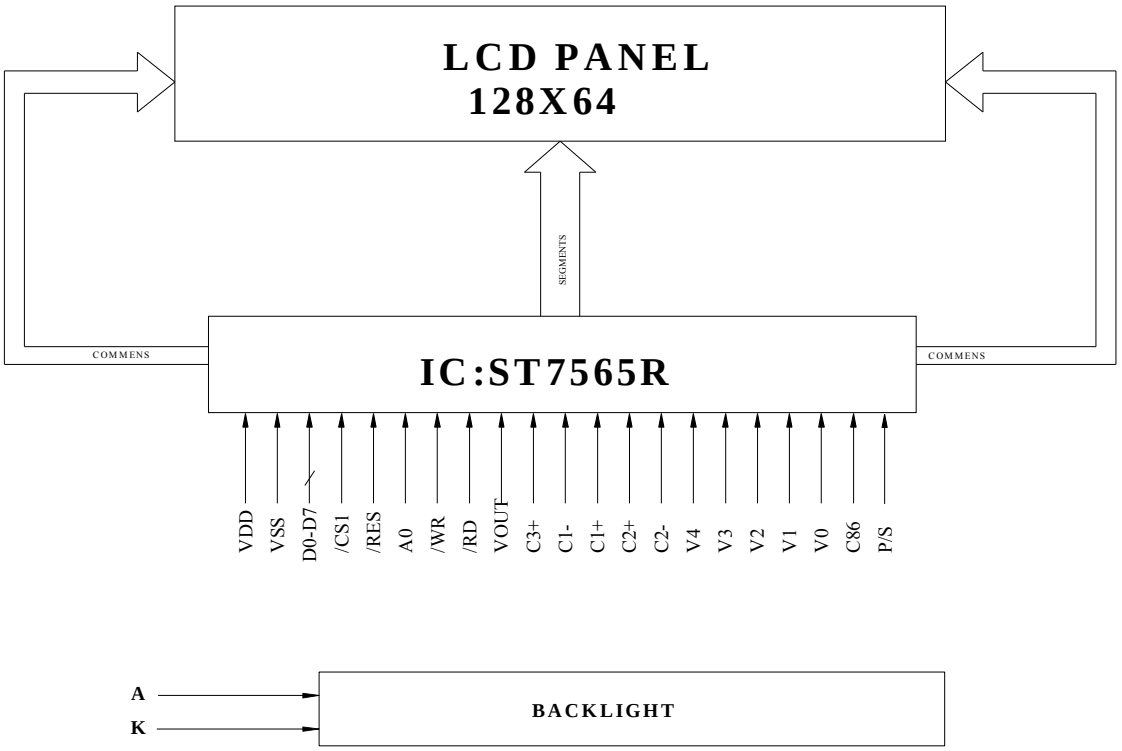
2. MECHANICAL SPECIFICATIONS

- Outline Dimensions : 77.40(W) x 52.40(L) x 6.50(H)(mm)
- Viewing Area : 70.00 (W) x 40.00(L)(mm)
- Active Area : 66.52 (W) x 33.24 (L)(mm)
- Dot Pitch : 0.52 (W) x 0.52 (L)(mm)
- Dot Size : 0.48 (W) x 0.48 (L)(mm)
- Weight : 35mg

3. EXTERNAL DIMENSIONS



4. BLOC`K DIAGRAM



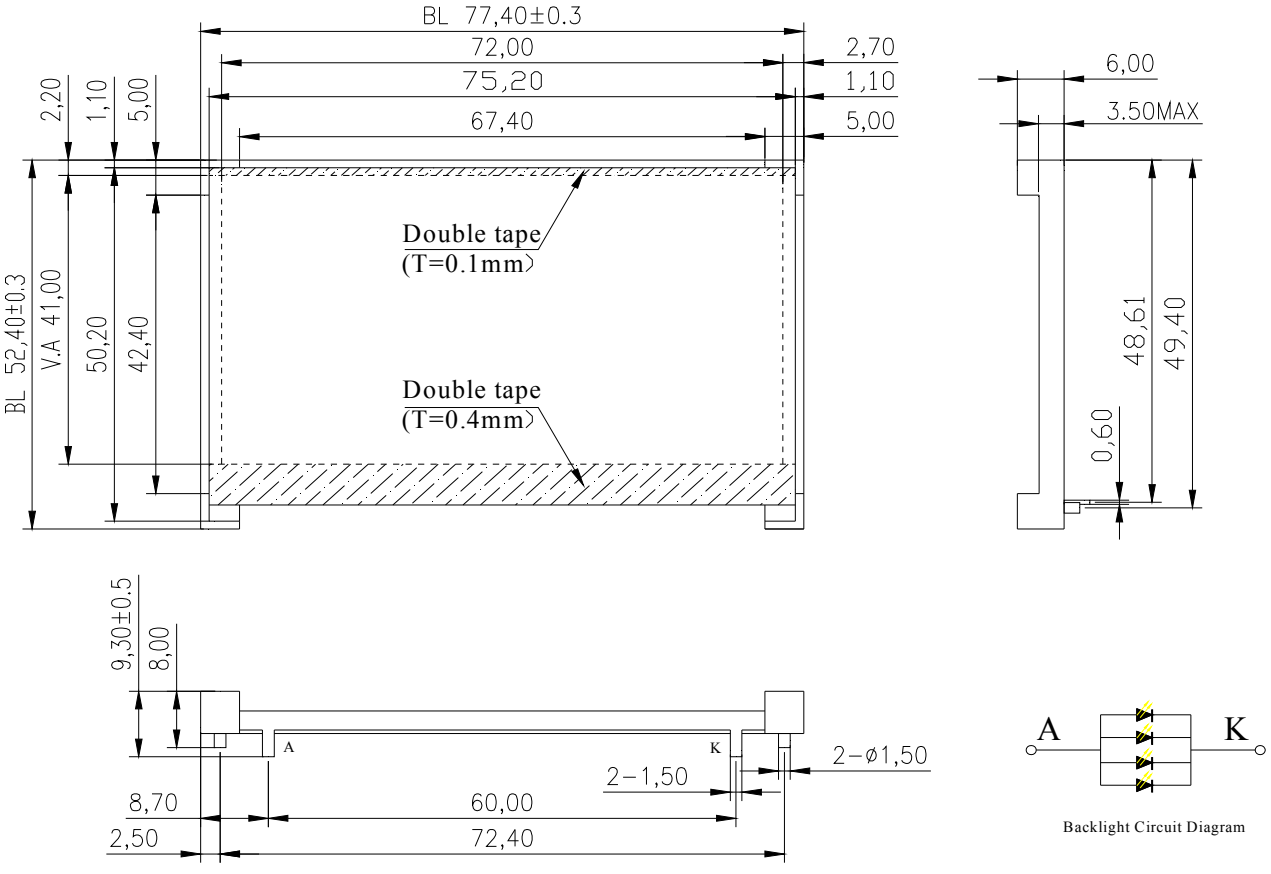
5. PIN ASSIGNMENT

Pin No.	Symbol	Function
1	/CS1	This is the chip select signal.
2	/RES	When /RES is set to “L”, the register settings are initialized (cleared). The reset operation is performed by the /RES signal level.
3	A0	This is connect to the least significant bit of the normal MPU address bus, and it determines whether the data bits are data or command. A0 = “H”: Indicates that D0 to D7 are display data. A0 = “L”: Indicates that D0 to D7 are control data.
4	/WR(R/W)	• When connected to 8080 series MPU, this pin is treated as the “/WR” signal of the 8080 MPU and is LOW-active. The signals on the data bus are latched at the rising edge of the /WR signal. • When connected to 6800 series MPU, this pin is treated as the “R/W” signal of the 6800 MPU and decides the access type : When R/W = “H”: Read. When R/W = “L”: Write.
5	/RD(E)	• When connected to 8080 series MPU, this pin is treated as the “/RD” signal of the 8080 MPU and is LOW-active. The data bus is in an output status when this signal is “L”. • When connected to 6800 series MPU, this pin is treated as the “E” signal of the 6800 MPU and is HIGH-active. This is the enable clock input terminal of the 6800 Series MPU.
6-13	D0-D7	This is an 8-bit bi-directional data bus that connects to an 8-bit or 16-bit standard MPU data bus. When the serial interface (SPI-4) is selected (P/S = “L”) : D7: serial data input (SI) ; D6 : the serial clock input (SCL). D0 to D5 should be connected to VDD or floating. When the chip select is not active, D0 to D7 are set to high impedance.
14	VDD	Power terminal of module
15	VSS	Ground terminal of module.
16	VOUT	DC/DC voltage converter. Connect a capacitor between this terminal and VSS or VDD terminal.
17	CAP3P	DC/DC voltage converter. Connect a capacitor between this terminal and the CAP3P terminal.
18	CAP1N	DC/DC voltage converter. Connect a capacitor between this terminal and the CAP1N terminal.
19	CAP1P	DC/DC voltage converter. Connect a capacitor between this terminal and the CAP1P terminal.
20	CAP2P	DC/DC voltage converter. Connect a capacitor between this terminal and the CAP2P terminal.
21	CAP2N	DC/DC voltage converter. Connect a capacitor between this terminal and the CAP2N terminal.
22	V4	This is a multi-level power supply for the liquid crystal drive. The voltage Supply applied is determined by the liquid crystal cell, and is changed through the use of a resistive voltage divided or through changing the impedance using an op. amp. Voltage levels are determined based on Vss, and must maintain the relative magnitudes shown below. V0 ≧V1 ≧V2 ≧V3 ≧V4 ≧Vss
23	V3	
24	V2	
25	V1	
26	V0	
27	C86	This is the MPU interface selection pin. C86 = “H”: 6800 Series MPU interface. C86 = “L”: 8080 Series MPU interface.
28	P/S	This pin configures the interface to be parallel mode or serial mode. P/S = “H”: Parallel data input/output. P/S = “L”: Serial data input.
	A	Anode of Backlight
	K	Cathode of Backlight

6. BACKLIGHT ELECTRICAL/OPTICAL SPECIFICATIONS

Electrical/Optical Specifications

ITEM	SYMBOL	MIN.	TYP.	MAX.	UNIT	CONDITIONS
Forward Voltage	Vf	2.9	3.1	3.3	V	If= 15 x4 mA
Reverse Current	Ir			120	mA	Vr=5.0 V
Power Dissipation	Pd			275	mW	If= 15 x4 mA
Dominant wave length	X		0.299	0.33		If= 15 x 4 mA
	Y		0.313	0.33	-	
Luminous	Lv	220	250		cd/m^2	If= 15 x 4 mA
Luminous Uniformity	△Lv	70			%	If= 15 x 4 mA



NOTES :

1. Unmarked tolerance is ±0.2
2. All materials comply with RoHS
3. Color: White
4. 4 PCS LEDS

7. MAXIMUM ABSOLUTE POWER RATINGS

Item	Symbol	Standard value	Unit
Power supply voltage(1)	V_{DD}	-0.3~+3.6	V
Power supply voltage(2)	$V_{OUT,,}$ $V_{0,}$	-0.3 ~ 13.5	V
Power supply voltage(3)	V_{IN}	-0.3 ~ V0	V
Operating temperature	Topr	-20~+70	℃
Storage temperature	Tstg	-30~+80	℃

*Voltage greater than above may damage to the Circuit.

Vout＞V0＞V1＞V2＞V3＞V4

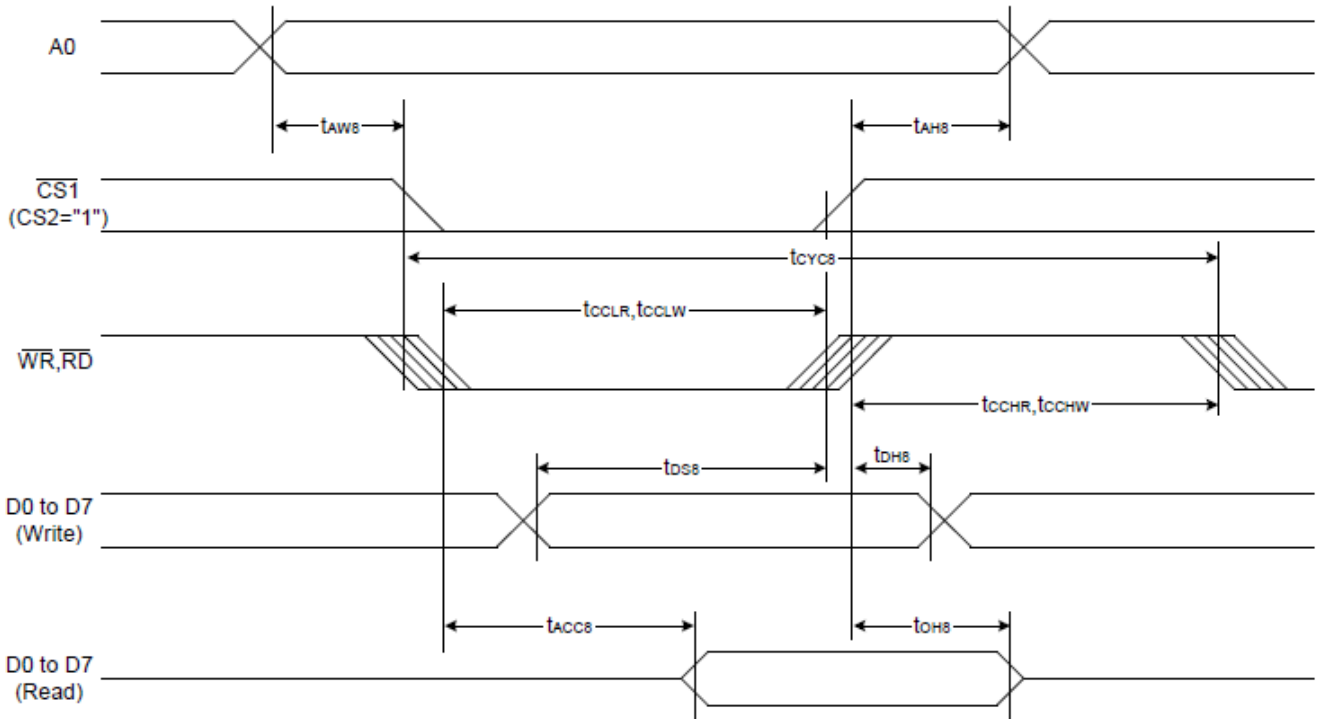
8. ELECTRICAL CHARACTERISTICS

8-1 DC Characteristics

Item	Symbol	Standard Value			Test Condition	Unit
		Min	Typ	Max		
Operating Voltage	V_{DD} -Vss	2.8	3.0	3.2	TA=25℃	V
Supply Current	I_{DD}	----	TBD	5.0	--	mA
LCD Driving Voltage	V_0-V_{ss}	8.8	9.0	9.2	TA=25℃	V

8-2 AC Characteristics

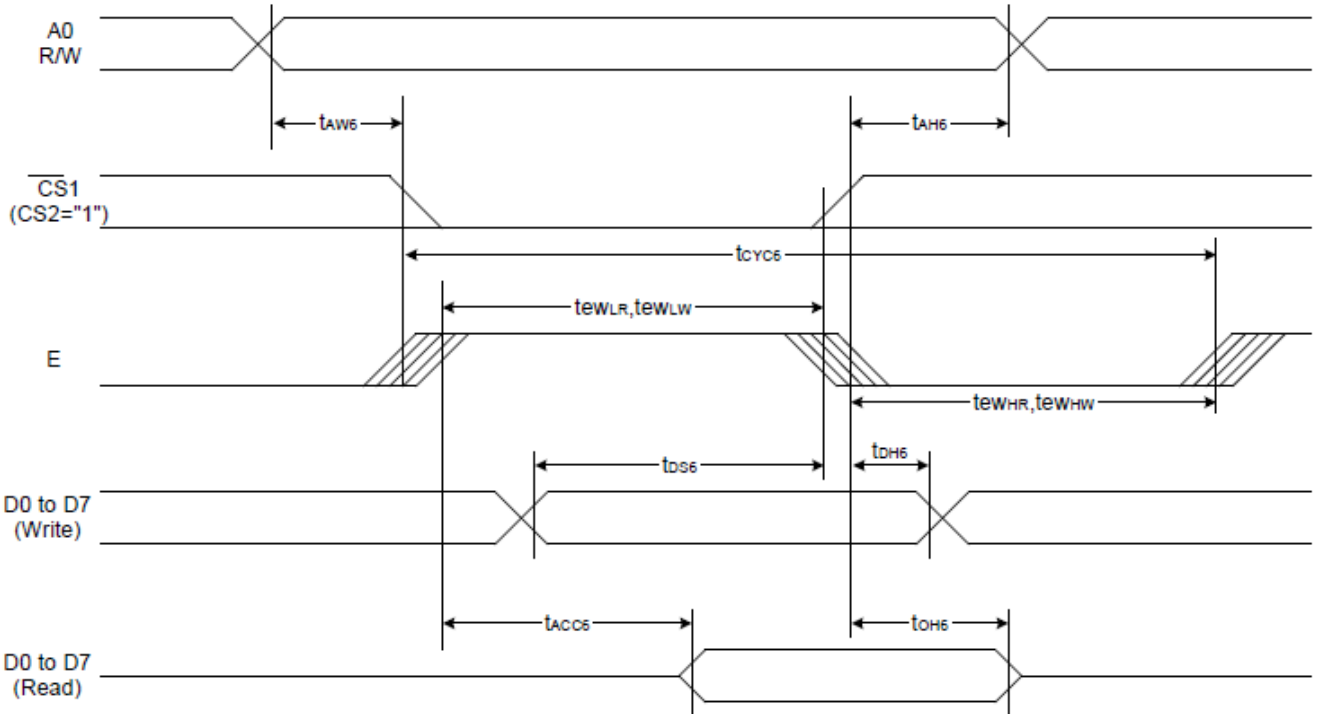
8.2.1 Read/Write mode for the 8080 Series MPU



Item	Signal	Symbol	Condition	Rating		Units
				Min.	Max.	
Address hold time	A0	t_{AH8}		0	—	Ns
Address setup time		t_{AW8}		0	—	
System cycle time		t_{CYC8}		240	—	
Enable L pulse width (WRITE)	WR	t_{CCLW}		80	—	
Enable H pulse width (WRITE)		t_{CCHW}		80	—	
Enable L pulse width (READ)	RD	t_{CCLR}		140	—	
Enable H pulse width (READ)		t_{CCHR}		80		
WRITE Data setup time	D0 to D7	t_{DS8}		40	—	
WRITE Address hold time		t_{DH8}		0	—	
READ access time		t_{ACC8}	C_L = 100 pF	—	70	
READ Output disable time		t_{OH8}	C_L = 100 pF	5	50	

*1 The input signal rise time and fall time (t_r, t_f) is specified at 15 ns or less. When the system cycle time is extremely fast, ($t_r + t_f$) ≦ ($t_{CYC8} - t_{CCLW} - t_{CCHW}$) for ($t_r + t_f$) ≦ ($t_{CYC8} - t_{CCLR} - t_{CCHR}$) are specified.
*2 All timing is specified using 20% and 80% of V_{DD} as the reference.
*3 t_{CCLW} and t_{CCLR} are specified as the overlap between /CS1 being "L" (CS2 = "H") and /WR and /RD being at the "L" level.

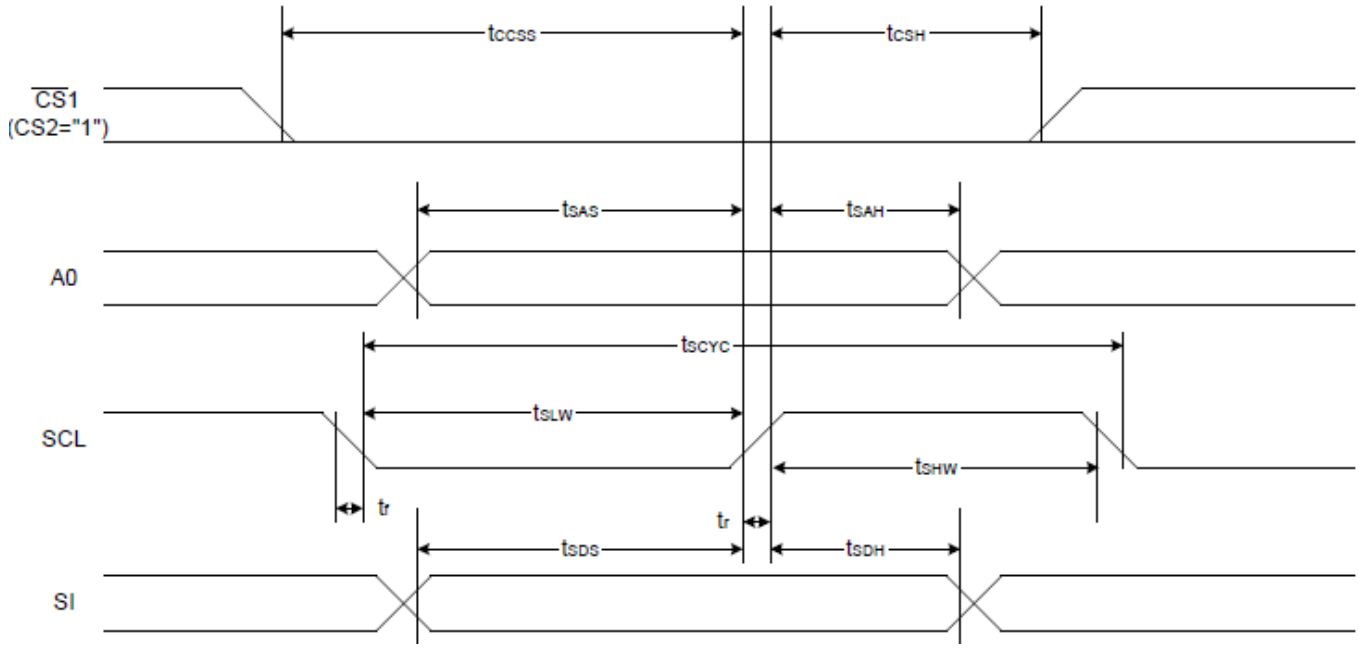
8.2.2 Read/Write mode for the 6800 Series MPU



Item	Signal	Symbol	Condition	Rating		Units
				Min.	Max.	
Address hold time	A0	t_{AH6}		0	—	ns
Address setup time		t_{AW6}		0	—	
System cycle time		t_{CYC6}		240	—	
Enable L pulse width (WRITE)	WR	t_{EWLW}		80	—	
Enable H pulse width (WRITE)		t_{EWHW}		80	—	
Enable L pulse width (READ)	RD	t_{EWLR}		80	—	
Enable H pulse width (READ)		t_{EWHR}		140		
WRITE Data setup time	D0 to D7	t_{DS6}		40	—	
WRITE Address hold time		t_{DH6}		0	—	
READ access time		t_{ACC6}	C_L = 100 pF	—	70	
READ Output disable time		t_{OH6}	C_L = 100 pF	5	50	

*1 The input signal rise time and fall time (t_r, t_f) is specified at 15 ns or less. When the system cycle time is extremely fast, ($t_r + t_f$) ≦ ($t_{CYC6} - t_{EWLW} - t_{EWHW}$) for ($t_r + t_f$) ≦ ($t_{CYC6} - t_{EWLR} - t_{EWHR}$) are specified.
*2 All timing is specified using 20% and 80% of V_{DD} as the reference.
*3 t_{EWLW} and t_{EWLR} are specified as the overlap between $\overline{CS1}$ being "L" (CS2 = "H") and E.

8.2.3 The 4-line SPI Interface



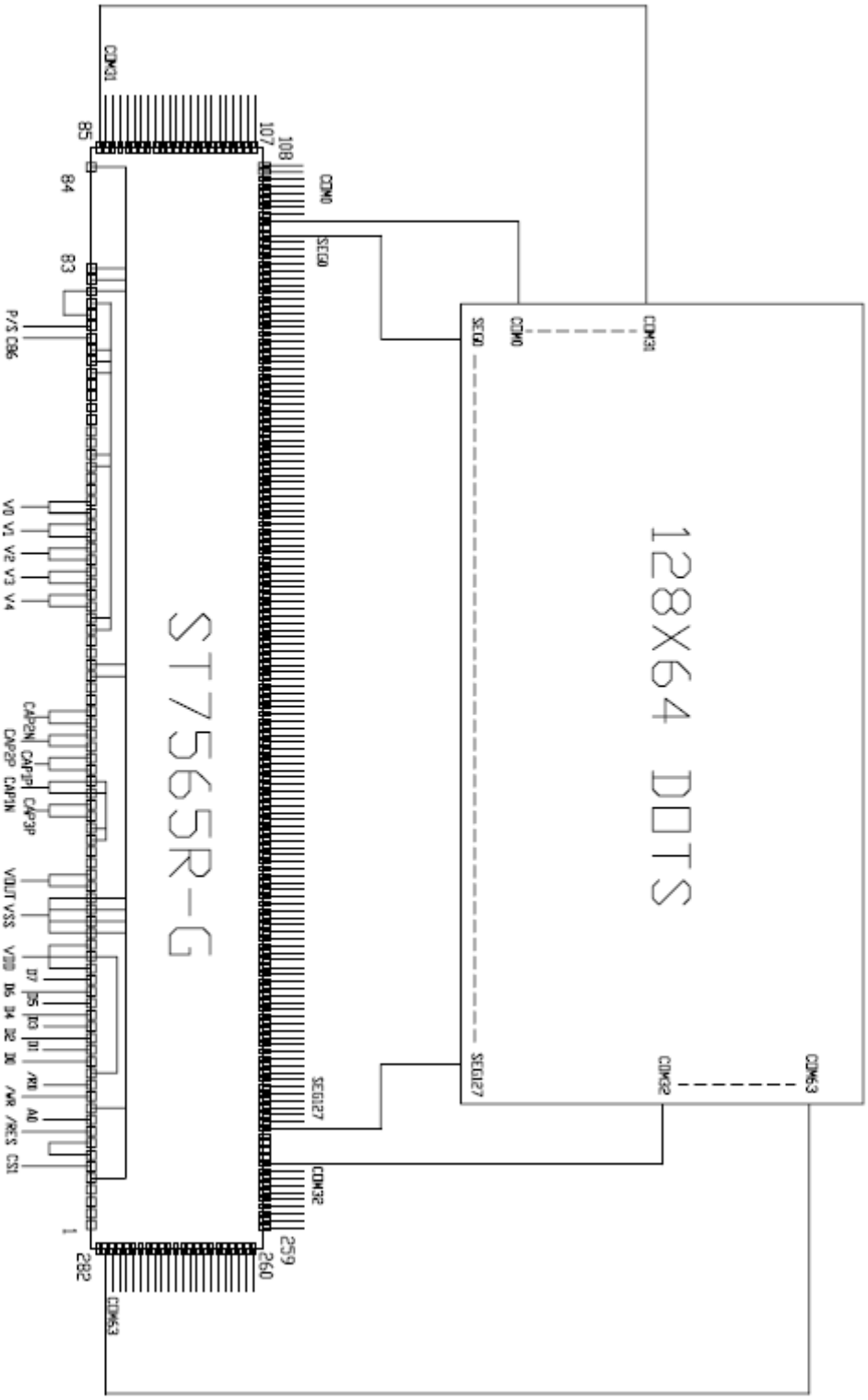
Item	Signal	Symbol	Condition	Rating		Units
				Min.	Max.	
4-line SPI Clock Period	SCL	T_{scyc}		50	—	ns
SCL "H" pulse width		T_{shw}		25	—	
SCL "L" pulse width		T_{SLW}		25	—	
Address setup time	A0	T_{SAS}		20	—	
Address hold time		T_{sah}		10	—	
Data setup time	SI	T_{sds}		20	—	
Data hold time		T_{SDH}		10	—	
CS-SCL time	CS	T_{css}		20	—	
CS-SCL time		T_{csh}		40	—	

9. INSTRUCTION TABLE

Table of ST7565P Commands (Note) *: disabled data

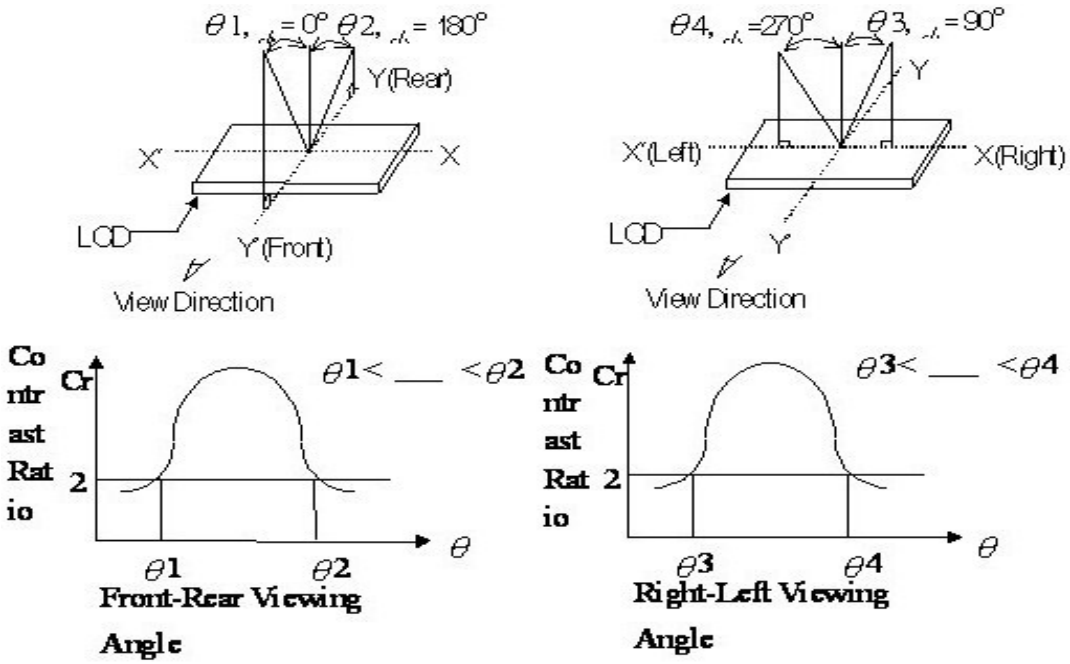
Command	Command Code										Function
	A0	/RD	/WR	D7	D6	D5	D4	D3	D2	D1	D0	
(1) Display ON/OFF	0	1	0	1	0	1	0	1	1	1	0 1	LCD display ON/OFF 0: OFF, 1: ON
(2) Display start line set	0	1	0	0	1	Display start address						Sets the display RAM display start line address
(3) Page address set	0	1	0	1	0	1	1	Page address				Sets the display RAM page address
(4) Column address set upper bit Column address set lower bit	0 0	1 1	0 0	0 0	0 0	0 0	1 0	Most significant column address Least significant column address				Sets the most significant 4 bits of the display RAM column address. Sets the least significant 4 bits of the display RAM column address.
(5) Status read	0	0	1	Status				0	0	0	0	Reads the status data
(6) Display data write	1	1	0	Write data								Writes to the display RAM
(7) Display data read	1	0	1	Read data								Reads from the display RAM
(8) ADC select	0	1	0	1	0	1	0	0	0	0	0 1	Sets the display RAM address SEG output correspondence 0: normal, 1: reverse
(9) Display normal/ reverse	0	1	0	1	0	1	0	0	1	1	0 1	Sets the LCD display normal/ reverse 0: normal, 1: reverse
(10) Display all points ON/OFF	0	1	0	1	0	1	0	0	1	0	0 1	Display all points 0: normal display 1: all points ON
(11) LCD bias set	0	1	0	1	0	1	0	0	0	1	0 1	Sets the LCD drive voltage bias ratio 0: 1/9 bias, 1: 1/7 bias (ST7565P)
(12) Read/modify/write	0	1	0	1	1	1	0	0	0	0	0	Column address increment At write: +1 At read: 0
(13) End	0	1	0	1	1	1	0	1	1	1	0	Clear read/modify/write
(14) Reset	0	1	0	1	1	1	0	0	0	1	0	Internal reset
(15) Common output mode select	0	1	0	1	1	0	0	0 1	*	*	*	Select COM output scan direction 0: normal direction 1: reverse direction
(16) Power control set	0	1	0	0	0	1	0	1	Operating mode			Select internal power supply operating mode
(17) V0 voltage regulator internal resistor ratio set	0	1	0	0	0	1	0	0	Resistor ratio			Select internal resistor ratio(Rb/Ra) mode
(18) Electronic volume mode set Electronic volume register set	0	1	0	1 0	0 0	0 Electronic volume value	0	0	0	0	1	Set the V0 output voltage electronic volume register
(19) Static indicator ON/OFF Static indicator register set	0	1	0	1 0	0 0	1 0	0 0	1 0	1 0	0 0	0 1 Mode	0: OFF, 1: ON Set the flashing mode
(20) Booster ratio set	0	1	0	1 0	1 0	1 0	1 0	1 0	0 0	0 step-up value	0	select booster ratio 00: 2x,3x,4x 01: 5x 11: 6x
(21) Power saver												Display OFF and display all points ON compound command
(22) NOP	0	1	0	1	1	1	0	0	0	1	1	Command for non-operation
(23) Test	0	1	0	1	1	1	1	*	*	*	*	Command for IC test. Do not use this command

10. IC LAYOUT

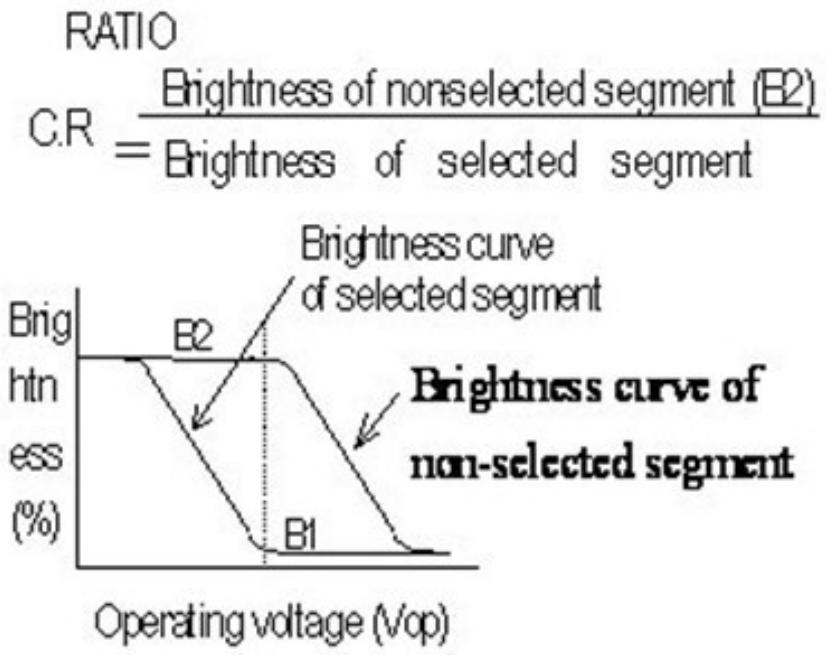

ST7565R-G
128X64 DOTS
COM0
COM63
SEG0
SEG127
P/S
C86
V0
V1
V2
V3
V4
CAP2N
CAP1P
CAP2P
CAP3P
CAP1N
VOUT
VSS
VDD
D7
D6
D5
D4
D3
D2
D1
D0
/RD
/WR
A0
/RES
CS1
84
83
85
107
108
259
260
282
1

11. Optical Characteristics

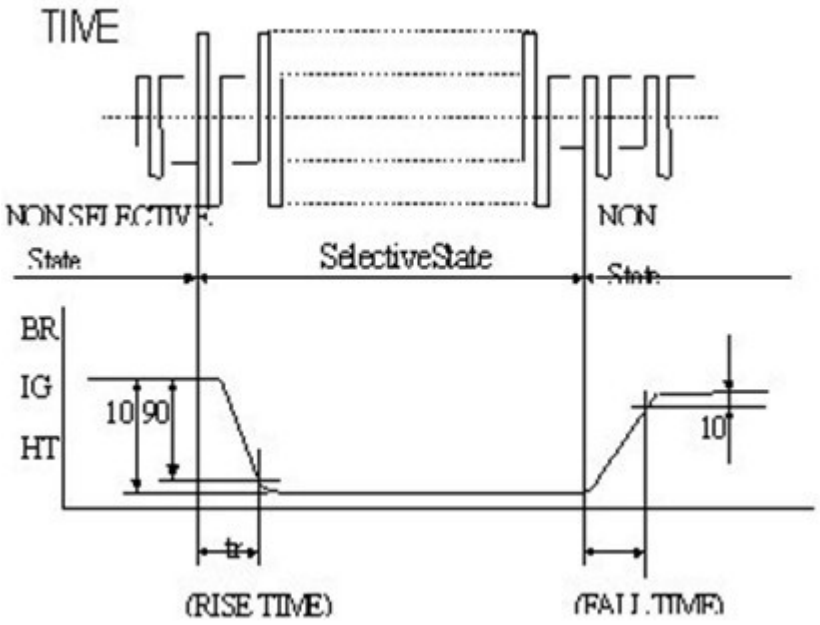
11.1 Definition of Viewing Angle



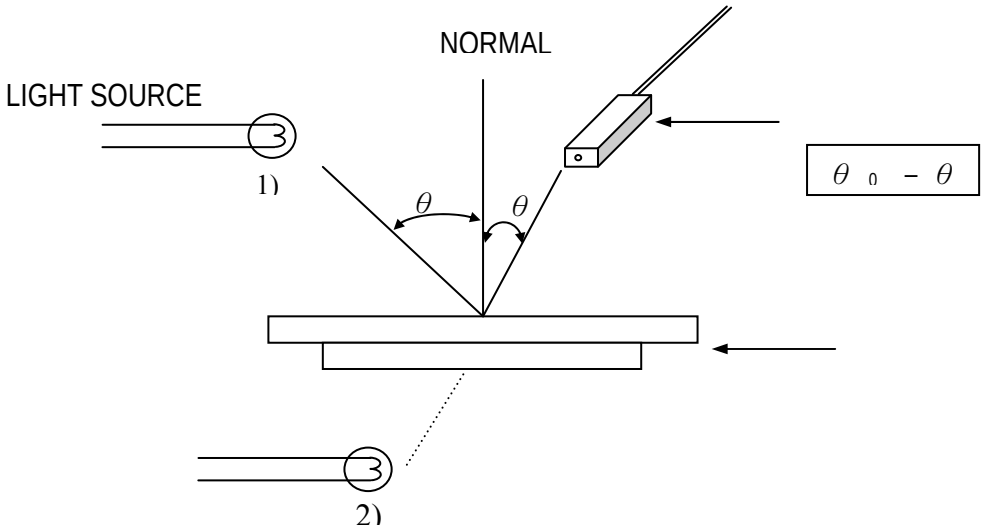
11.2 Definition of Contrast



11.3 Definition of Response



11.4 Measuring Instruments For Electro-optical Characteristics



*** Note:**

1) Light source position for measuring the reflective type of LCD panel;
2) Light source position for measuring the transflective / transmissive types of LCD panel.

12. MODULE ACCEPT QUALITY LEVEL (AQL)

12.1 AQL Standard Value: Critical Defect =0.1, Major Defect=0.65; Minor Defect =2.5.
12.2 Inspection Standard: MIL-STD-105E Table Normal Inspection Single Sampling Level II

13. RELIABILITY TEST

Operating life time: Longer than 50,000 hours
(at room temperature without direct irradiation of sunlight)
Reliability characteristics shall meet following requirements.

No.	Test Item	Content of Test	Test Condition
1	High Temperature Storage	Endurance test applying the high storage temperature for a long time	+80°C 96H
2	Low Temperature Storage	Endurance test applying the low storage temperature for a long time	−30°C 96H
3	High Temperature Operation	Endurance test applying the electric stress (voltage & current) and the thermal stress to the element for a long time	+70°C 96H
4	Low Temperature Operation	Endurance test applying the electric stress under low temperature for a long time	−20°C 96H
5	High Temperature/ Humidity Storage	Endurance test applying the high temperature and humidity storage for a long time	60°C 90%RH 96H
6	Temperature Cycle	Endurance test applying the low and high temperature cycle −20°C ⟷ 25°C ⟷ 70°C ⟷ 25°C 30min 5min 30min 5min ⟷ 1 cycle	−20°C/70°C 5 cycles
7	Vibration Test (Package State)	Endurance test applying the vibration during transportation	10Hz－55Hz, 50m/s, 15min
8	Shock Test (Package State)	Endurance test applying the shock during transportation	Half-sinewave, 100m/s, 11ms
9	Atmospheric Pressure Test	Endurance test applying the atmospheric pressure during transportation by air	40 kPa 16 H

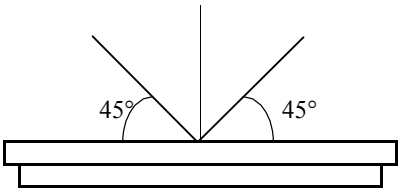
14. Packaging

TBD

15. Inspection specification

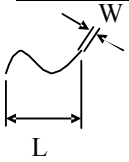
15.1 Visual Inspection

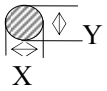
1) Inspect under 2x20W or 40W fluorescent lamp (approximately 3000 lux) leaving 25 to 30 cm between the module and the lamp and 30 cm between the module and the eye (measuring position).
2) Appearance is inspected at the best contrast voltage (best contrast is adjusted considering clearness and crosstalk on screen).
3) Inspect the module at 45° right and left, top and bottom.
4) Use the optimum viewing angle during the contrast inspection.

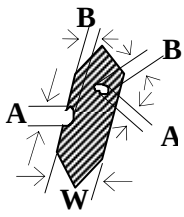


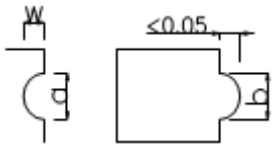
15.2 Standard of Appearance Inspection

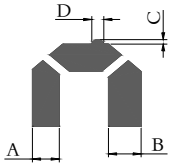
<table>
<tr><th>No.</th><th>Item</th><th>Criteria</th></tr>
<tr><td rowspan="2">1</td><td>Black spot
White spot
Dust</td><td>
Round type: as per following drawing
Φ = (X+Y)/2

X
<table>
<tr><td colspan="3">Acceptable quantity</td></tr>
<tr><td>Size</td><td>Zone A</td><td>Zone B</td></tr>
<tr><td>Φ <0.1</td><td>Any number</td><td rowspan="4">Any number</td></tr>
<tr><td>0.1< Φ <0.2</td><td>2</td></tr>
<tr><td>0.2< Φ <0.25</td><td>1</td></tr>
<tr><td>0.25< Φ</td><td>0</td></tr>
</table>
Line type: as per following drawing
<table>
<tr><td colspan="4">Acceptable quantity</td></tr>
<tr><td>Length</td><td>Width</td><td>Zone A</td><td>Zone B</td></tr>
<tr><td>—</td><td>W≤0.02</td><td>Any number</td><td rowspan="4">Any number</td></tr>
<tr><td>L≤3.0</td><td>0.02<W≤0.03</td><td rowspan="2">2</td></tr>
<tr><td>L≤2.5</td><td>0.03<W≤0.05</td></tr>
<tr><td>—</td><td>0.05<W</td><td>As round type</td></tr>
</table>

W
L
Total acceptable quantity: 3
</td></tr>
<tr><td>2</td><td>Polariser</td><td>Scratch on protective film is permitted</td></tr>
</table>

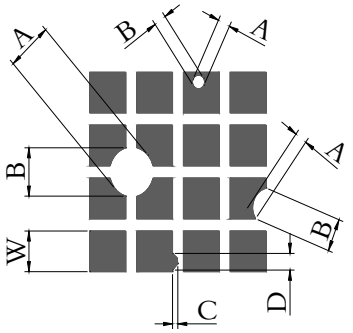
<table>
<tr><td></td><td>scratch</td><td>Scratch on polariser: same as No. 1</td></tr>
<tr><td>3</td><td>Polariser bubble</td><td>Φ = (X+Y)/2
 

Total acceptable quantity: 3
<table><tr><td colspan="3">Acceptable quantity</td></tr><tr><td>Size</td><td>Zone A</td><td>Zone B</td></tr><tr><td>Φ <0.2</td><td>Any number</td><td rowspan="4">Any number</td></tr><tr><td>0.2< Φ <0.5</td><td>2</td></tr><tr><td>0.5< Φ <1.0</td><td>1</td></tr><tr><td>1.0< Φ</td><td>0</td></tr></table></td></tr>
<tr><td>4</td><td>Segment deformation</td><td>4.1 Pin hole on segmented display
W: segment width
Φ = (A+B)/2
 

<table><tr><td colspan="2">Acceptable quantity</td></tr><tr><td>Width</td><td>Quantity</td></tr><tr><td>W≤0.4</td><td>Φ ≤0.2 and Φ ≤1/2W</td></tr><tr><td>W>0.4</td><td>Φ ≤0.25 and Φ ≤1/3W</td></tr><tr><td colspan="2">Total acceptable quantity: 1 defect per segment
Pin holes with Φ under 0.10 mm are acceptable</td></tr></table>
4.2 Pin hole on dot matrix display
 

Total acceptable quantity: 7
<table><tr><td colspan="2">Acceptable quantity</td></tr><tr><td>Size</td><td></td></tr><tr><td>a, b<0.1</td><td>Any number</td></tr><tr><td>(a+b)/2≤0.1</td><td>Any number</td></tr><tr><td>0.5< Φ <1.0</td><td>3</td></tr></table>
4.3 Segments / dots with different width
 

<table><tr><td colspan="2">Acceptable</td></tr><tr><td>a≥b</td><td>a/b≤4/3</td></tr><tr><td>a<b</td><td>a/b>4/3</td></tr></table>
4.4 Alignment layer defect</td></tr>
</table>

<table>
<tr><td></td><td></td><td>Φ = (A+B)/2
 

Total acceptable quantity: 7
<table><tr><td colspan="2">Acceptable quantity</td></tr><tr><td>Size</td><td></td></tr><tr><td>Φ ≤0.4</td><td>Any number</td></tr><tr><td>0.4< Φ ≤1.0</td><td>5</td></tr><tr><td>1.0< Φ ≤1.5</td><td>3</td></tr><tr><td>1.5< Φ ≤2.0</td><td>2</td></tr></table></td></tr>
<tr><td>5</td><td>Colour uniformity</td><td>Level of sample for approval set as limit sample</td></tr>
<tr><td>6</td><td>Backlight</td><td>The backlight colour should correspond to the product specification
Flashing and or unlit backlight is not allowed
Dust larger than 0.25 mm is not allowed</td></tr>
<tr><td>7</td><td>COB</td><td>Exposed wire bond pad is not allowed
Insufficient covering with resin is not allowed (wire bond line exposed) Dust or bubble on the resin are not allowed</td></tr>
<tr><td>8</td><td>PCB</td><td>No unmelted solder paste should be present on PCB
Cold solder joints, missing solder connections, or oxidation are not allowed
No residue or solder balls on PCB are allowed
Short circuits on components are not allowed</td></tr>
<tr><td>9</td><td>Tray particles</td><td><table><tr><td colspan="3">Acceptable quantity</td></tr><tr><td></td><td>Size</td><td>Quantity</td></tr><tr><td rowspan="2">On tray</td><td>Φ <0.2</td><td>Any number</td></tr><tr><td>Φ >0.25</td><td>4</td></tr><tr><td>On display</td><td>Φ ⩾0.25</td><td>2</td></tr><tr><td></td><td>L = 3</td><td>1</td></tr></table></td></tr>
</table>

16. LCD MODULES HANDLING PRECAUTIONS

- Please remove the protection foil of polarizer before using.
- The display panel is made of glass. Do not subject it to a mechanical shock by dropping it from a high place, etc.

- If the display panel is damaged and the liquid crystal substance inside it leaks out, do not get any in your mouth. If the substance come into contact with your skin or clothes promptly wash it off using soap and water.

- Do not apply excessive force to the display surface or the adjoining areas since this may cause the color tone to vary.

- The polarizer covering the display surface of the LCD module is soft and easily scratched. Handle this polarize carefully.

- To prevent destruction of the elements by static electricity, be careful to maintain an optimum work environment.
  -Be sure to ground the body when handling the LCD module.
  -Tools required for assembly, such as soldering irons, must be properly grounded.
  -To reduce the amount of static electricity generated, do not conduct assembly and other work under dry conditions.
  -The LCD module is coated with a film to protect the display surface. Exercise care when peeling off this protective film since static electricity may be generated.

- Storage precautions
  When storing the LCD modules, avoid exposure to direct sunlight or to the light of fluorescent lamps. Keep the modules in bags designed to prevent static electricity charging under low temperature / normal humidity conditions (avoid high temperature / high humidity and low temperatures below 0 ℃).Whenever possible, the LCD modules should be stored in the same conditions in which they were shipped from our company.

17. OTHERS

- Liquid crystals solidify at low temperature (below the storage temperature range) leading to defective orientation of liquid crystal or the generation of air bubbles (black or white). Air bubbles may also be generated if the module is subjected to a strong shock at a low temperature.

- If the LCD modules have been operating for a long time showing the same display patterns may remain on the screen as ghost images and a slight contrast irregularity may also appear. Abnormal operating status can be resumed to be normal condition by suspending use for some time. It should be noted that this phenomena does not adversely affect performance reliability.

- To minimize the performance degradation of the LCD modules resulting from caused by static electricity, etc. exercise care to avoid holding the following sections when handling the modules:
  - Exposed area of the printed circuit board
  - Terminal electrode sections