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8051-Based MCU

MG82F6D17
Datasheet

Version: 0.38

Features

- 1-T 80C51 Central Processing Unit
- **MG82F6D17** with **16K** Bytes flash ROM
  - ISP memory zone could be optioned as **0.5KB/1.0KB~7.5KB**
  - Flexible IAP size by software configured
  - Code protection for flash memory access
  - Flash write/erase cycle: 20,000
  - Flash data retention: 100 years at 25°C
- **Default MG82F6D17 Flash space mapping**
  - AP Flash default mapping (13.5KB, 0000h~35FFh)
  - IAP Flash default mapping (1.0KB, 3600h~39FFh)
  - ISP Flash default mapping (1.5KB, 3A00h~3FFFh), ISP Boot code
- Data RAM: **1K** Bytes
  - On-chip 256 bytes scratch-pad RAM
  - **768** bytes expanded RAM (XRAM) for **MG82F6D17**
  - Support page select on XRAM access in **MG82F6D17**
- Dual data pointer
- Provide one channel DMA engine
  - P2P, M2P, P2M
  - Memory target: XRAM
  - Peripheral target: UART0, UART1, SPI, TWI0/I2C0, ADC12 & CRC16
  - Timer 5 and Timer 6 are used for DMA, but it also can be traded as independent timer when DMA not in use
- Interrupt controller
  - **16** sources, four-level-priority interrupt capability
  - **Three** external interrupt inputs, nINT0, nINT1 and nINT2 with glitch filter
  - All external interrupts support High/Low level or Rising/Falling edge trigger
- Total **9/11** timers in **MG82F6D17**
  - RTC Timer and WDT Timer
  - Timer 0, Timer 1, Timer 2 and Timer 3
  - PCA0, Program Counter Array 0
  - S0 BRG and S1 BRG
  - If Timer 2/3 in split mode, total **11** timers
- **Four** 16-bit timer/counters, Timer 0, Timer 1, Timer 2 and Timer 3
  - X12 mode and timer clock output function
  - Synchronous Run-Enable on all timer (same function on Stop and Reload)
  - New 5 operating modes in Timer 2/3 with 8 clock sources and 8 capture sources
  - Timer 2/3 can be split to two 8-bit timers
  - Clock Count Output (CCO) on T2CKO and T3CKO
  - All timers support PWM mode
- **One** Programmable 16-bit counter/timer Arrays (PCA0) with **8** Compare/PWM modules
  - PCA0 has 6 CCP (Capture/Compare/PWM) modules and 2 CP (Compare/PWM) modules
  - Reloadable 16-bit base counter to support variable length PWM
  - Up to **144 MHz** clock source from on-chip CKM
  - Capture mode, 16-bit software timer mode and High speed output mode
  - Buffered capture mode to monitor narrow pulse input
  - Variable 8/10/12/16-bit PWM mode, the PCA can be configured to:
    - Up to **8** channels un-buffered 10/12/16-bit PWM, or

  - ∗ Up to **8** channels buffered 2~8-bit PWM, or
  - ∗ Up to **4** channels buffered 9~16-bit PWM
- — PCA0 PWM module 0~5 with dead-time control, break control and central-aligned option

- 8 Inputs Keypad Interrupt
- 12-Bit Single-ended ADC
  - — Programmable throughput up to **800K** sps
  - — 8 channel external inputs and one channel internal input (IVR/1.4V)
  - — Support window detect function on ADC result
  - — Support channel scan mode
- Enhanced UART (S0)
  - — Framing Error Detection
  - — Automatic Address Recognition
  - — Max. UART baud rate up to 3.6864MHz/ 6MHz
  - — Support SPI Master in Mode 4, up to 12MHz on SPICLK
  - — Built-in baud rate generator (S0BRG) to support TX or RX on different baud rate
  - — Support LIN bus protocol with auto baud rate detection in mode 5
  - — S0BRG in timer mode cascaded with Timer 0/1 to be a 16/24-bit timer/counter
- Secondary UART (S1)
  - — Dedicated Baud Rate Generator (S1BRG) shares to S0 or set as an 8-bit timer
  - — Max. UART baud rate up to 1.8432/3.0MHz
  - — Support SPI Master in Mode 4, up to 12MHz on SPICLK
  - — S1BRG in timer mode cascaded with Timer 0/1 to be a 16/24-bit timer/counter
- One Master/Slave SPI serial interface
  - — Max. 24MHz (V_{DD} > 3.3V), 16MHz (V_{DD} = 1.8V) SPICLK on SPI master
  - — Max 12MHz on SPI slave
  - — 8 bits data transfer
  - — Up to 3 SPI masters including S0/S1 in mode 4
  - — Support daisy-chain function in SPI slave mode
- Two Master/Slave two wire serial interfaces: TWI0/ I2C0 and STWI (SI2C)
  - — One Master/Slave hardware engine: TWI0/ I2C0
  - — Max. 1MHz on TWI0/ I2C0 master mode and Max. 400KHz on TWI0 slave mode
  - — One software TWI/ I2C, STWI/ SI2C, Start/Stop serial interface detection (SID)
- Programmable Watchdog Timer (WDT), clock sourced from ILRCO or SYSCLK
  - — One time enabled by CPU or power-on
  - — Interrupt CPU or Reset CPU on WDT overflow
  - — Support WDT function in power down mode (watch mode) for auto-wakeup function
- Real-Time-Clock (RTC) module, clock sourced from ILRCO, WDTPS, WDTOF, SYSCLK or SYSCLK/12
  - — Programmable interrupt period from mini-second wakeup to minute wakeup
  - — 21-bit length system timer
- Beeper function
- General purpose logic (GPL/CRC)
  - — Bit order reversed function
  - — 16-bit CRC engine (CCITT-16 polynomial)
  - — Support automatic CRC of flash content
  - — Programmable initial seed function of CRC
- On-Chip-Debug interface (OCD)
  - — **MG82F6D17AS8** SOP8 not support OCD
- Maximum **17** GPIOs in 20-pin package
  - — P3 can be configured to quasi-bidirectional, push-pull output, open-drain output and input only
  - — P0, P1, P2, P4 and P6 can be configured to open-drain output or push-pull output

  - P4.7 shared with RST
  - Programmable GPIO driving strength and driving speed
  - On chip pull-up enabled on each pin
- Clock Sources
  - Internal 12MHz/11.059MHz oscillator (IHRCO): factory calibrated to ±1%, typical
  - Internal Low power 32KHz RC Oscillator (ILRCO)
  - External clock input (ECKI) on P6.0, up to 25MHz
  - Internal RC Oscillator output on P6.0
  - On-chip Clock Multiplier (CKM) to provide high speed clock source (144 MHz)
- Two Brown-Out Detectors
  - BOD0: detect **1.7V**
  - BOD1: selected detection level on 4.2V/3.7V/2.4V/2.0V
  - Interrupt CPU or reset CPU
  - Wake up CPU in Power-Down mode (BOD1)
- Multiple power control modes: idle mode, power-down mode, slow mode, sub-clock mode, RTC mode, watch mode and monitor mode.
  - All interrupts can wake up IDLE mode
  - **12(13)** sources with **16** pins to wake up Power-Down mode
  - Slow mode and sub-clock mode support low speed MCU operation
  - RTC mode supports RTC to resume CPU in power down
  - Watch mode supports WDT to resume CPU in power down
  - Monitor mode supports BOD1 to resume CPU in power down
- Operating voltage range: 1.8V – 5.5V
  - Minimum **1.8V** requirement in flash write operation (ISP/IAP/ICP)
- Operation frequency range: **32** (max)
  - External clock input mode, 0 – 12MHz @ 2.0V – 5.5V, 0 – 25MHz @ 2.4V – 5.5V
  - CPU up to 12MHz @ **1.8V** – 5.5V, and up to 25MHz @ **2.2V** – 5.5V
  - **CPU up to 36MHz @ 2.7V -5.5V with on-chip CKM**
- 16-Bytes Unique ID code
- Operating Temperature:
  - Industrial (-40°C to +105°C)*
- Package Types:
  - SOP8 (150 mil): MG82F6D17AS8 (16K)
  - SSOP20 (150 mil): MG82F6D17AL20 (16K)
  - TSSOP20 (173 mil): MG82F6D17AT20 (16K)
  - QFN20 (3 x 3 x 0.55 mm): MG82F6D17AZ20 (16K)
  - PDIP20 (300mil): MG82F6D17AE20 (16K)

*: Tested by sampling.

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1. General Description

The **MG82F6D17** is a single-chip microcontroller based on a high performance 1-T architecture 80C51 CPU that executes instructions in 1~7 clock cycles (about 6~7 times the rate of a standard 8051 device), and has an 8051 compatible instruction set. Therefore at the same performance as the standard 8051, the **MG82F6D17** can operate at a much lower speed and thereby greatly reduce the power consumption.

The **MG82F6D17** has **16K** bytes of embedded Flash memory for code and data. The Flash memory can be programmed either in serial writer mode (via ICP, In-Circuit Programming) or in In-System Programming mode. And, it also provides the In-Application Programming (IAP) capability. ICP and ISP allow the user to download new code without removing the microcontroller from the actual end product; IAP means that the device can write non-volatile data in the Flash memory while the application program is running. There needs no external high voltage for programming due to its built-in charge-pumping circuitry.

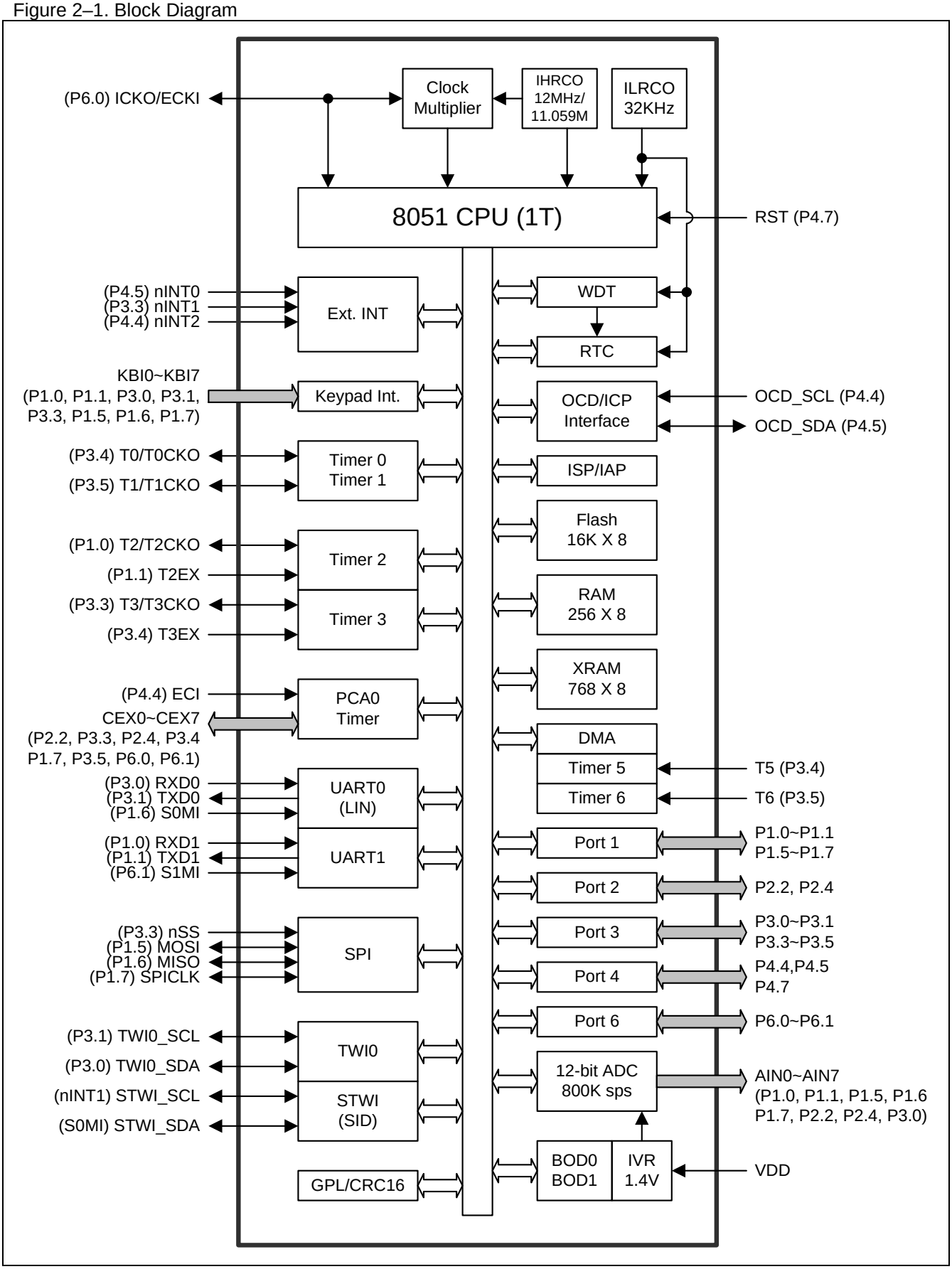
The **MG82F6D17** retains all features of the standard 80C52 with 256 bytes of scratch-pad RAM, two external interrupts, a multi-source 4-level interrupt controller, a serial port (UART0) and three timer/counters. In addition, the **MG82F6D17** has17 I/O port pins, one XRAM of 768 bytes, one extra external interrupts with High/low trigger option, 800KHz 12-bit ADC, one 16-bit timer, one 8-channel PCA with dead-time controlled PWM, one 8-bit SPI, two TWI/ I2C (TWI0/ I2C0 and STWI/ SI2C), secondary serial port (UART1), keypad interrupt, Watchdog Timer, Real-Time-Clock module, two Brown-out Detectors, an ECKI external clock input (P6.0), an internal high precision oscillator (IHRCO), an on-chip clock multiplier (CKM) to generate high speed clock source, an internal low speed RC oscillator (ILRCO) and an enhanced serial function in UART0 that facilitates multiprocessor communication, LIN bus mode and a speed improvement mechanism (X2/X4 mode). Support 3 different DMA transfer types, M2P (XRAM to Peripheral), P2M (Peripheral to XRAM) and P2P (Peripheral to Peripheral) to enhance transfer performance and reduce CPU loading.

The **MG82F6D17** has multiple operating modes to reduce the power consumption: idle mode, power down mode, slow mode, sub-clock mode, RTC mode, watch mode and monitor mode. In the Idle mode the CPU is frozen while the peripherals and the interrupt system are still operating. In the Power-Down mode the RAM and SFRs' value are saved and all other functions are inoperative; most importantly, in the Power-down mode the device can be waked up by many interrupt or reset sources. In slow mode, the user can further reduce the power consumption by using the 8-bit system clock pre-scaler to slow down the operating speed. Or select sub-clock mode which clock source is derived from internal low speed oscillator (ILRCO) for CPU to perform an ultra-low speed operation. The RTC module supports Real-Time-Clock function in all operating modes. In watch mode, it keeps WDT running in power-down or idle mode and resumes CPU as an auto-wakeup timer when WDT overflows. Monitor mode provides the Brown-Out detection in power down mode and resumes CPU when chip VDD reaches the specific detection level.

Additionally, the **MG82F6D17** is equipped with the Megawin proprietary On-Chip Debug (OCD) interface for In-Circuit Emulator (ICE). The OCD interface provides on-chip and in-system non-intrusive debugging without any target resource occupied. Several operations necessary for an ICE are supported such as Reset, Run, Stop, Step, Run to Cursor and Breakpoint Setting. The user has no need to prepare any development board during firmware developing or the socket adapter used in the traditional ICE probe head. All the thing the user needs to do is to prepare a connector for the dedicated OCD interface. This powerful feature makes the developing very easy for any user.

2. Block Diagram

Figure 2–1. Block Diagram



3. Pin Configurations

3.1. Package Instruction

Figure 3–1. SSOP20 Top View

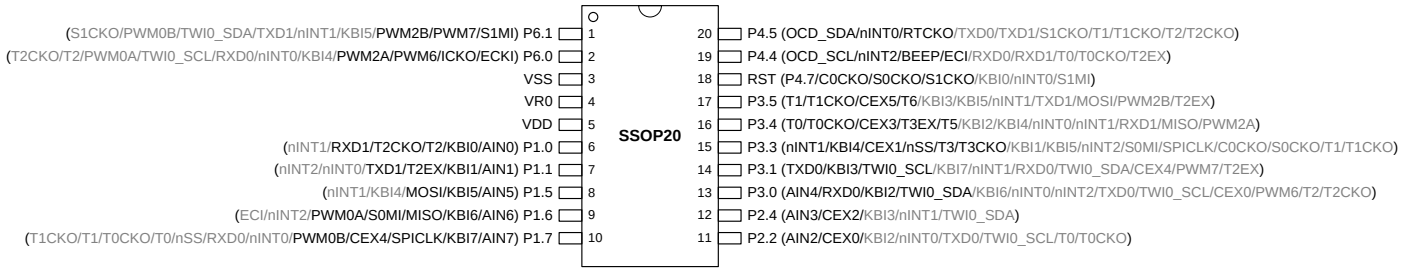


Figure 3–2. TSSOP20 Top View

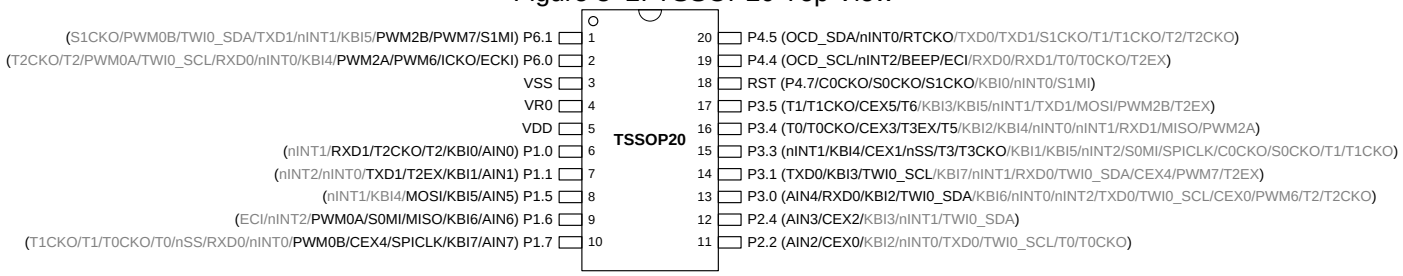


Figure 3–3. PDIP20 Top View

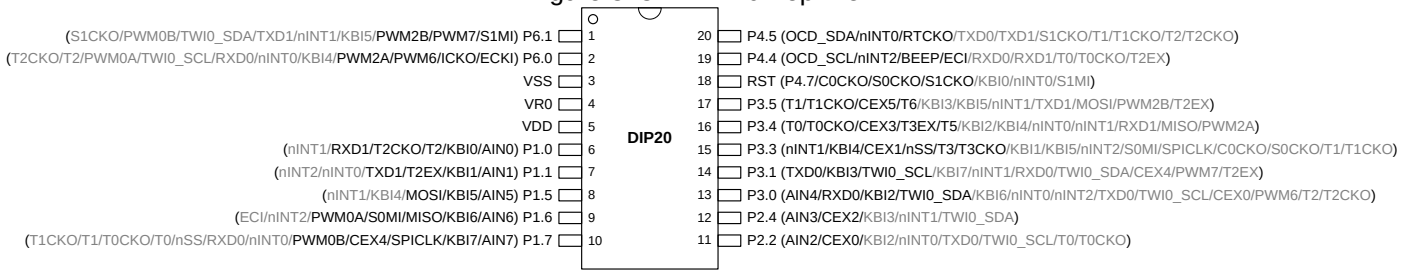


Figure 3–4. QFN20 Top View

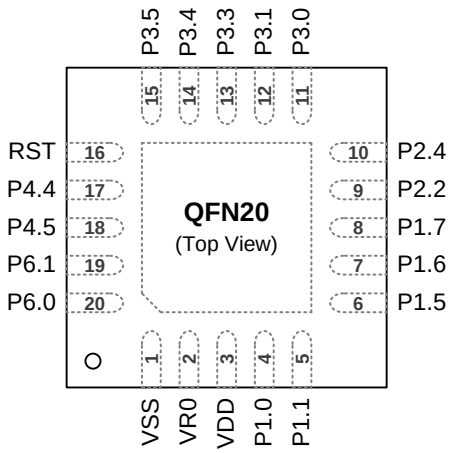
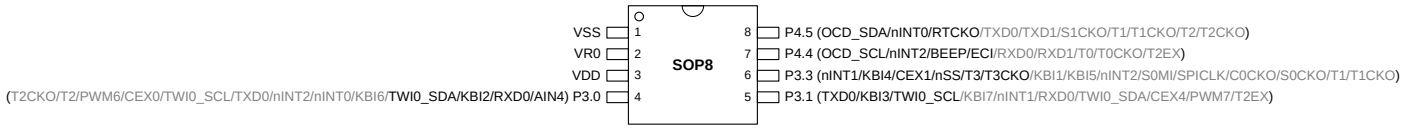


Figure 3–5. SOP8 Top View



Note: For MG82F6D17AS8 SOP8

1. *Does not support OCD ICE or ICP, reference "32.3 ICP and OCD Interface Circuit" for detail.*
2. *P4.4 and P4.5 is used for OCD function as default mode, please disable OCD_ICE in the initial step of the firmware.*

3.2. Pin Description

Table 4–1. Pin Description

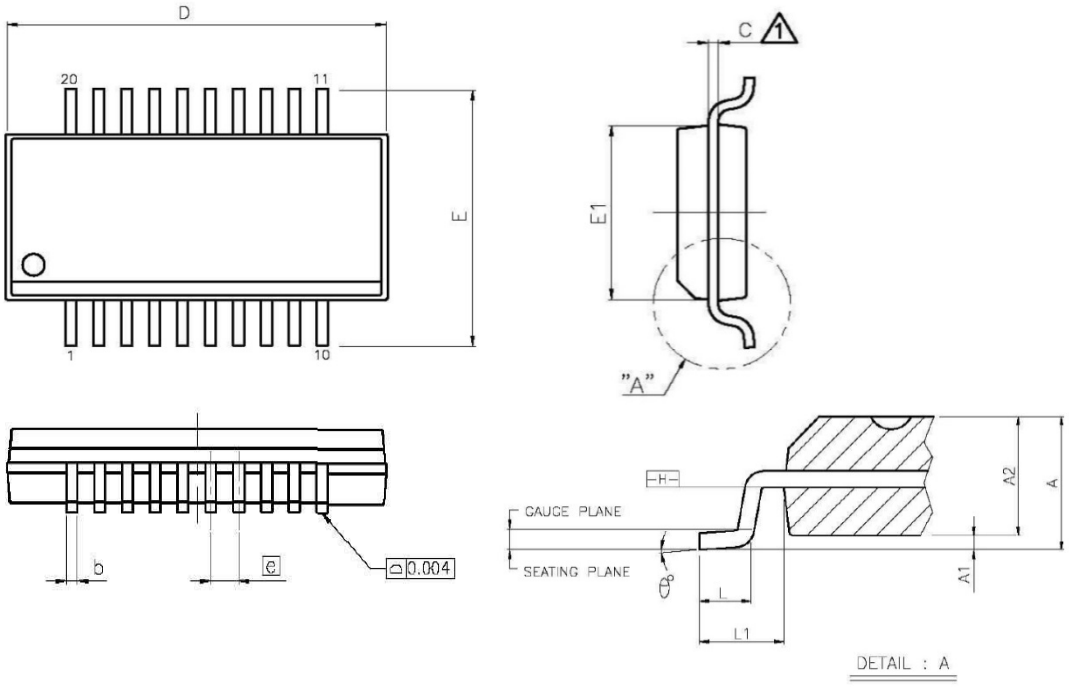
MNEMONIC	PIN NUMBER					I/O TYPE	DESCRIPTION
	20-Pin SSOP	20-Pin TSSOP	20-Pin PDIP	20-Pin QFN	8-Pin SOP		
P1.0 (AIN0) (KBI0) (T2) (T2CKO) (RXD1)	6	6	6	4		I/O	* Port 1.0. * AIN0: ADC channel-0 analog input. * KBI0: keypad input 0. * T2: Timer/Counter 2 external clock input. * T2CKO: Timer 2 programmable clock output. * RXD1: UART1 serial input port.
P1.1 (AIN1) (KBI1) (T2EX) (TXD1)	7	7	7	5		I/O	* Port 1.1. * AIN1: ADC channel-1 analog input. * KBI1: keypad input 1. * T2EX: Timer/Counter 2 external control input. * TXD1: UART1 serial output port.
P1.5 (AIN5) (KBI5) (MOSI)	8	8	8	6		I/O	* Port 1.5. * AIN5: ADC channel-5 analog input. * KBI5: keypad input 5. * MOSI: SPI master out & slave in.
P1.6 (AIN6) (KBI6) (MISO) (S0MI) (PWM0A)	9	9	9	7		I/O	* Port 1.6. * AIN6: ADC channel-6 analog input. * KBI6: keypad input 6. * MISO: SPI master in & slave out. * S0MI: Serial Port 0 SPI Master mode data Input. * PWM0A: PCA PWM0 output sub-channel A.
P1.7 (AIN7) (KBI7) (SPICLK) (CEX4) (PWM0B)	10	10	10	8		I/O	* Port 1.7. * AIN7: ADC channel-7 analog input. * KBI7: keypad input 7. * SPICLK: SPI clock, output for master and input for slave. * CEX4: PCA0 module-4 external I/O. * PWM0B: PCA0 PWM0 output sub-channel B.
P2.2 (AIN2) (CEX0)	11	11	11	9		I/O	* Port 2.2. * AIN2: ADC channel-2 analog input. * CEX0: PCA0 module-0 external I/O.
P2.4 (AIN3) (CEX2)	12	12	12	10		I/O	* Port 2.4. * AIN3: ADC channel-3 analog input. * CEX2: PCA0 module-2 external I/O.
P3.0 (AIN4) (RXD0) (KBI2) (TWI0_SDA)	13	13	13	11	4	I/O	* Port 3.0. * AIN4: ADC channel-4 analog input. * RXD0 : UART0 serial input port. * KBI2: keypad input 2. * TWI0_SDA: serial data of TWI0/ I2C0.
P3.1 (TXD0) (KBI3) (TWI0_SCL)	14	14	14	12	5	I/O	* Port 3.1. * TXD0 : UART0 serial output port. * KBI3: keypad input 3. * TWI0_SCL: serial clock of TWI0/ I2C0.
P3.3 (nINT1) (KBI4) (CEX1) (nSS) (T3) (T3CKO)	15	15	15	13	6	I/O	* Port 3.3. * nINT1: external interrupt 1 input. * KBI4: keypad input 4. * CEX1: PCA0 module-1 external I/O. * nSS: SPI Slave select. * T3: Timer/Counter 3 external clock input. * T3CKO: Timer 3 programmable clock output.
P3.4 (T0) (T0CKO) (CEX3) (T3EX) (T5)	16	16	16	14		I/O	* Port 3.4. * T0: Timer/Counter 0 external input. * T0CKO: Timer 0 programmable clock output. * CEX3: PCA0 module-3 external I/O. * T3EX: Timer/Counter 3 external control input. * T5: Timer/Counter 5 external clock input.

MNEMONIC	PIN NUMBER					I/O TYPE	DESCRIPTION
	20-Pin SSOP	20-Pin TSSOP	20-Pin PDIP	20-Pin QFN	8-Pin SOP		
P3.5 (T1) (T1CKO) (CEX5) (T6)	17	17	17	15		I/O	* Port 3.5. * T1: Timer/Counter 1 external input. * T1CKO: Timer 1 programmable clock output. * CEX5: PCA0 module-5 external I/O. * T6: Timer/Counter 6 external clock input.
P4.4 (OCD_SCL) (nINT2) (BEEP) (ECI)	19	19	19	17	7	I/O	* Port 4.4. * OCD_SCL: OCD interface, serial clock. (Need to disable by firmware of MG82F6D17AS8 SOP8) * nINT2: external interrupt 2 input. * BEEP: Beeper output. * ECI: PCA external clock input.
P4.5 (OCD_SDA) (nINT0) (RTCKO)	20	20	20	18	8	I/O	* Port 4.5. * OCD_SDA: OCD interface, serial data. (Need to disable by firmware of MG82F6D17AS8 SOP8) * nINT0: external interrupt 0 input. * RTCKO: RTC programmable clock output.
P6.0 (ECKI) (ICKO) (PWM6) (PWM2A)	2	2	2	20		I/O I O	* Port 6.0. * ECKI: In external clock input mode, this is clock input pin. * ICKO: Internal Clock (MCK) Output. * PWM6: PCA0 module-6 PWM6 output. * PWM2A: PCA0 PWM2 output sub-channel A.
P6.1 (S1MI) (PWM7) (PWM2B)	1	1	1	19		I/O	* Port 6.1. * S1MI: Serial Port 1 SPI Master mode data Input. * PWM7: PCA0 module-7 PWM7 output. * PWM2B: PCA0 PWM2 output sub-channel B.
RST (P4.7) (C0CKO) (S0CKO) (S1CKO)	18	18	18	16		I I/O	* RST: External RESET input, high active. * Port 4.7. * C0CKO: Programmable clock output of PCA base counter. * S0CKO: S0BRT programmable clock output. * S1CKO: S1BRG programmable clock output.
VR0	4	4	4	2	2	I/O	* VR0. Voltage Reference 0. Connect 0.1uF and 4.7uF to VSS.
VDD	5	5	5	3	3	P	Power supply input.
VSS	3	3	3	1	1	G	Ground, 0 V reference.

4. Package Dimension

4.1. SSOP-20(150 mil) Dimension

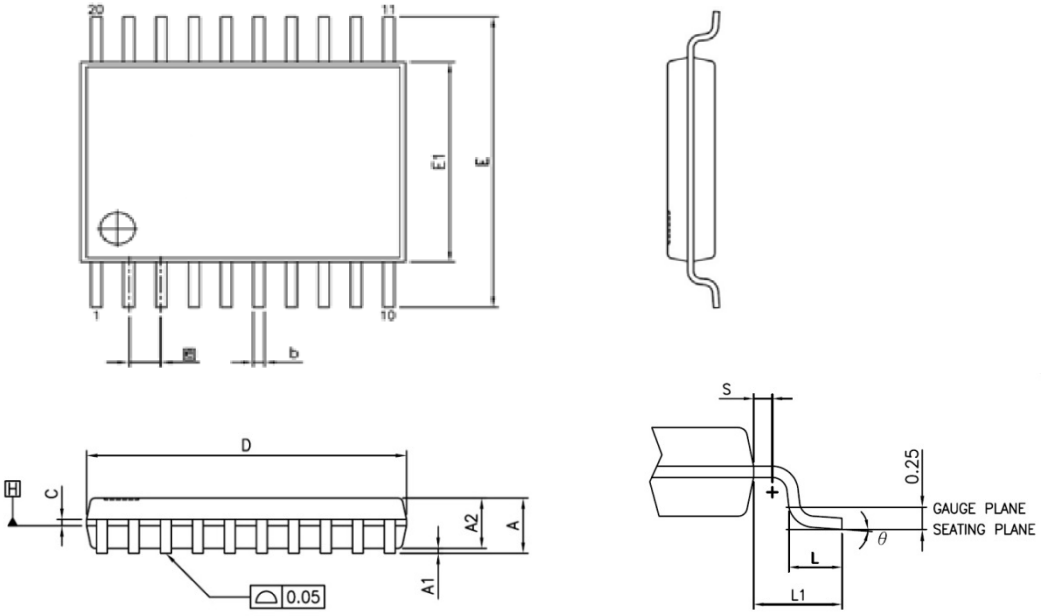
Figure 4-1. SSOP-20 (150 mil) Package Dimension



Unit	mm			inch		
Symbols	Min.	Nom.	Max.	Min.	Nom.	Max.
A	1.346	1.625	1.752	0.053	0.064	0.069
A1	0.101	0.152	0.254	0.004	0.006	0.010
A2	----	----	1.498	----	----	0.059
b	0.203	----	0.304	0.008	----	0.012
C	0.177	----	0.254	0.007	----	0.010
D	8.559	8.661	8.737	0.337	0.341	0.344
E	5.791	5.994	6.197	0.228	0.236	0.244
E1	3.810	3.911	3.987	0.150	0.154	0.157
e	0.635 BASIC			0.025 BASIC		
L	0.406	0.635	1.270	0.016	0.025	0.050
L1	1.041 BASIC			0.040 BASIC		
θ	0°	----	8°	0°	----	8°

4.2. TSSOP-20(173 mil) Dimension

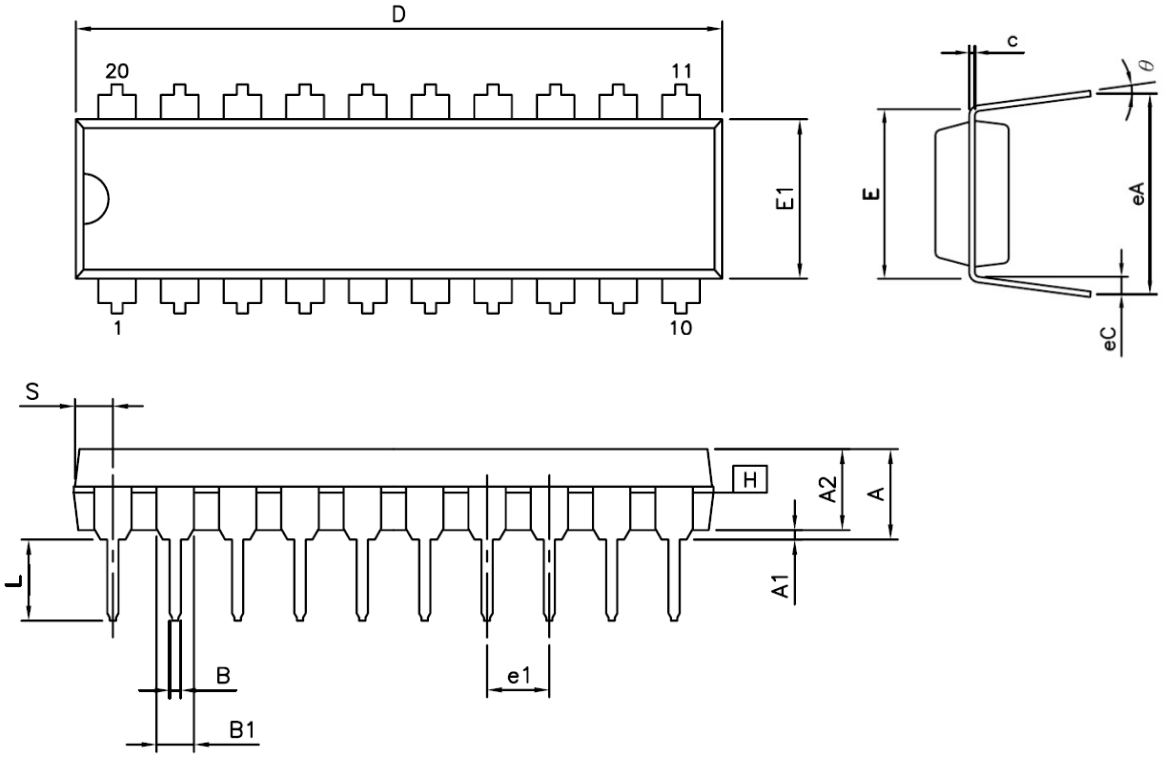
Figure 4-2. TSSOP-20 6.5 x 4.4mm, 0.65mm pitch Package Dimension



Unit	mm			inch		
Symbols	Min.	Nom.	Max.	Min.	Nom.	Max.
A	----	----	1.20	----	----	0.047
A1	0.05	----	0.15	0.001	----	0.005
A2	0.80	0.90	1.05	0.031	0.035	0.041
b	0.19	----	0.30	0.007	----	0.011
C	0.09	-----	0.20	0.003	-----	0.007
D	6.40	6.50	6.60	0.251	0.255	0.259
E1	4.30	4.40	4.50	0.169	0.173	0.177
E	6.40 BSC			0.251 BSC		
e	0.65 BSC			0.025 BSC		
L1	1.00 REF			0.039 REF		
L	0.50	0.60	0.75	0.019	0.023	0.029
S	0.20	----	----	0.007	----	----
θ	0°	----	8°	0°	----	8°

4.3. PDIP-20(300 mil) Dimension

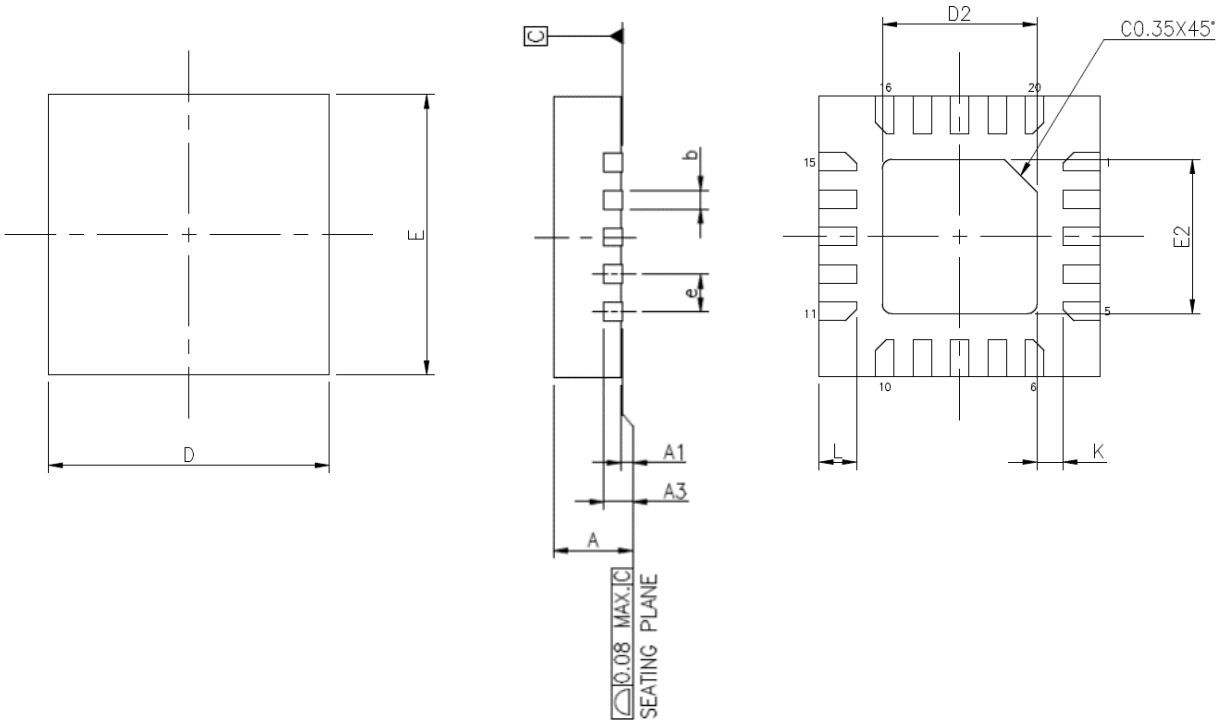
Figure 4-3. PDIP-20 (300 mil) Package Dimension



Unit	mm			inch		
Symbols	Min.	Nom.	Max.	Min.	Nom.	Max.
A	----	----	4.445	----	----	0.175
A1	0.381	----	----	0.015	----	----
A2	3.175	3.302	3.429	0.125	0.130	0.135
B	0.406	0.457	0.508	0.016	0.018	0.020
B1	1.473	1.524	1.549	0.058	0.060	0.061
c	0.203	0.254	0.279	0.008	0.010	0.011
D	25.704	26.060	26.416	1.012	1.026	1.040
E	7.620	----	7.874	0.300	----	0.310
E1	6.233	6.350	6.477	0.245	0.250	0.255
e 1	2.286	2.540	2.794	0.090	0.100	0.110
L	3.048	3.302	3.556	0.120	0.130	0.140
ɵ	0	----	381	0	----	15
eA	8.509	9.017	9.525	0.335	0.355	0.375
eC	0.000	----	1.524	0.000	----	0.060
S	----	----	1.905	----	----	0.075

4.4. QFN-20 (3x3x0.55mm) Package Dimension

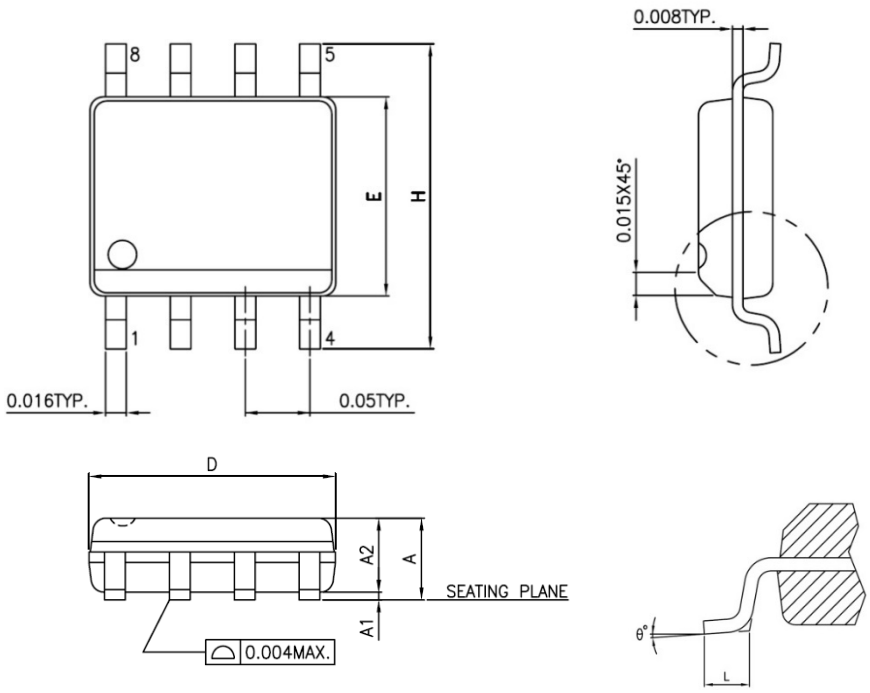
Figure 4-4. QFN-20 (3x3 x 0.55mm) Package Dimension



Unit	mm			inch		
JEDEC	MO-220			MO-220		
PKG	WQFN(X319)			WQFN(X319)		
Symbols	Min.	Nom.	Max.	Min.	Nom.	Max.
A	0.50	0.55	0.60	0.019	0.021	0.023
A1	0.00	0.02	0.05	0.000	0.000	0.001
A3	0.150 REF.			0.005 REF.		
b	0.15	0.20	0.25	0.005	0.007	0.009
D	3.00 BSC			0.11 BSC		
E	3.00 BSC			0.11 BSC		
e	0.40 BSC			0.015 BSC		
L	0.35	0.40	0.45	0.013	0.015	0.017
K	0.20	---	---	0.007	---	---
D2	1.60	1.65	1.70	0.062	0.064	0.066
E2	1.60	1.65	1.70	0.062	0.064	0.066

4.5. SOP-8 (150mil) Package Dimension

Figure 4-5. SOP-8 (150 mil) Package Dimension



Unit	mm		inch	
Symbols	Min.	Max.	Min.	Max.
A	1.346	1.752	0.052	0.068
A1	0.101	0.254	0.003	0.010
A2	1.346	1.498	0.052	0.058
D	4.800	4.978	0.188	0.195
E	3.810	3.987	0.150	0.156
H	5.791	6.197	0.227	0.243
L	0.406	1.270	0.015	0.050
θ	0°	8°	0	8

5. Revision History

Table 5–1. Revision History

Rev	Descriptions	Date
V0.35T	Initial version preliminary released	2019/03/18
V0.36T	1. Modified example of ADC Channel Scan Mode by DMA 2. Add IVR Characteristics 3. Fixed ADCFG0 Bit7~5 table description 4. Modified S0BRG description	2019/04/08
V0.37T	1. Modified ADC DMA description 2. Removed P6FDC, P6DC0 3. Add BME6 description 4. Modified DBSD[1:0] to DBSD 5. Modified CKMI output maximum frequency from 96MHz to 144MHz 6. Modified electrical characteristics 7. Modified ILRCO tolerance 8. Fixed error in SFR table, EPCnH to ECAPnH and EPCnL to ECAPnL 9. Modified HSE, HSE1 description 10. Added description on C0M0 11. Modified STOF, STAF description	2019/05/07
V0.38	1. Added SOP8 Package, and add ICP limitation description for SOP8 2. Added PDIP20 Package Dimension	2019/12/31

6. Disclaimers

Herein, Megawin stands for "***Megawin Technology Co., Ltd.***"

Life Support — This product is not designed for use in medical, life-saving or life-sustaining applications, or systems where malfunction of this product can reasonably be expected to result in personal injury. Customers using or selling this product for use in such applications do so at their own risk and agree to fully indemnify Megawin for any damages resulting from such improper use or sale.

Right to Make Changes — Megawin reserves the right to make changes in the products - including circuits, standard cells, and/or software - described or contained herein in order to improve design and/or performance. When the product is in mass production, relevant changes will be communicated via an Engineering Change Notification (ECN).